Millimeter-Wave Reconfigurable CMOS-MEMS Integrated Devices

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

The millimeter-wave spectrum has sparked interest recently as a promising alternative to meet bandwidth requirements for wireless local area networks, vehicular radars, short-range multi-Gb/s links, and next-generation cellular system communications (5G). The unlicensed 7 GHz ISM band around 60 GHz is of particular interest. Compared to semiconductor technologies, Micro-Electro-Mechanical Systems (MEMS) have the potential to realize reconfigurable millimeter-wave devices with superior performance in terms of linearity, insertion loss and DC power consumption.

This thesis presents the development and fabrication of miniaturized, low insertion loss, high isolation RF-MEMS switches implemented in CMOS chips through the use of a post-processing technique. Several CMOS-MEMS switches operating at 60 GHz and 77 GHz are demonstrated. Prototype units for SPST, SP3T switches and a distributed MEMS transmission line (DMTL) network are integrated on CMOS 0.35 μm. The challenges involved in realizing CMOS-MEMS devices at mm-wave frequencies are also addressed in this work.

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Dedication

To Akefeh and Jamshid.

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Introduction

1.1 Motivation

1.1.1 Why mm-wave?

Wireless local/personal area network (WLAN/WPAN) standards mostly operate in a few Gigahertz bands that are already heavily congested, and soon the emergence of new electronic devices will necessitate a move to free bands at higher frequencies. Numerous current and potential future applications demand short-range wireless communication requiring several hundreds of Mbps network capacity. For moderate spectral efficiency, such a high capacity could be provided only if a wide bandwidth of hundreds of MHz were available. This encourages the communication industry to take advantage of higher previously unallocated frequency ranges in the mm-wave region.

Due to their high propagation attenuation (i.e., free space path loss), mm-wave bands are desirable for secure short-range data transfer applications. The Friis formula states that the received-to-transmitted power ratio in terms of antenna directivities (D_1 and D_2), distance between points (R), and propagation wavelength (λ) would be: $\frac{P_r}{P_t} = \frac{D_1 D_2 \lambda^2}{(4\pi R)^2}$. This means merely scaling the frequency of operation from 6 to 60 GHz introduces a 20 dB loss. Moreover, there is extremely high absorption due to atmospheric oxygen, leading to 10-15 dB/km attenuation in a bandwidth of about 8 GHz centered at 60 GHz. Therefore, among mm-wave frequencies, the unlicensed industrial, scientific and medical (ISM) band around 60 GHz has gained attention worldwide as an option to service short-range high data rate applications.

For instance, the Wireless Gigabit Alliance, subsumed by the Wi-Fi Alliance, has aimed to move Wi-Fi from 2.4 GHz and 5 GHz to the 60 GHz band for short-range communication that is up to 10 times faster. Thus far, the so-called WiGig standard has developed short-distance (up to 10 m), high-speed (up to 7 Gbps) wireless data transfers at 60 GHz. Figure 1.1 shows the approved spectra around 60 GHz worldwide. As an example for potential applications, Figure 1.2 shows a scenario for a dual band system operating at 5 GHz and 60 GHz for wireless communication in an office or a home environment.

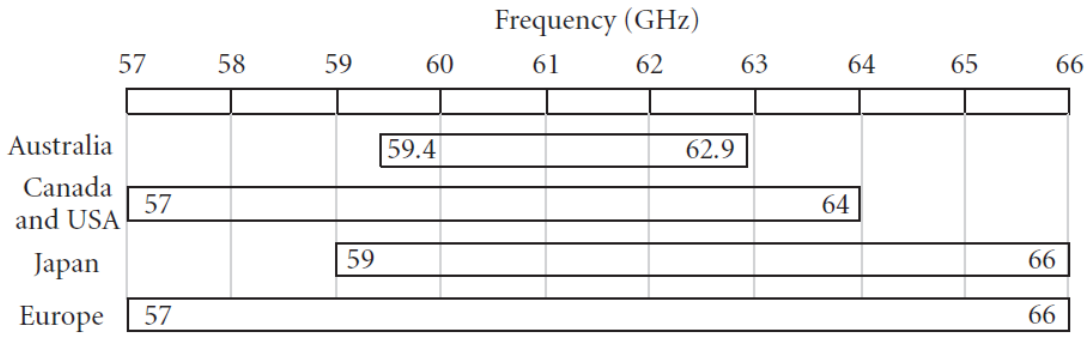


Figure 1-1: Available frequency range around 60 GHz worldwide [1].

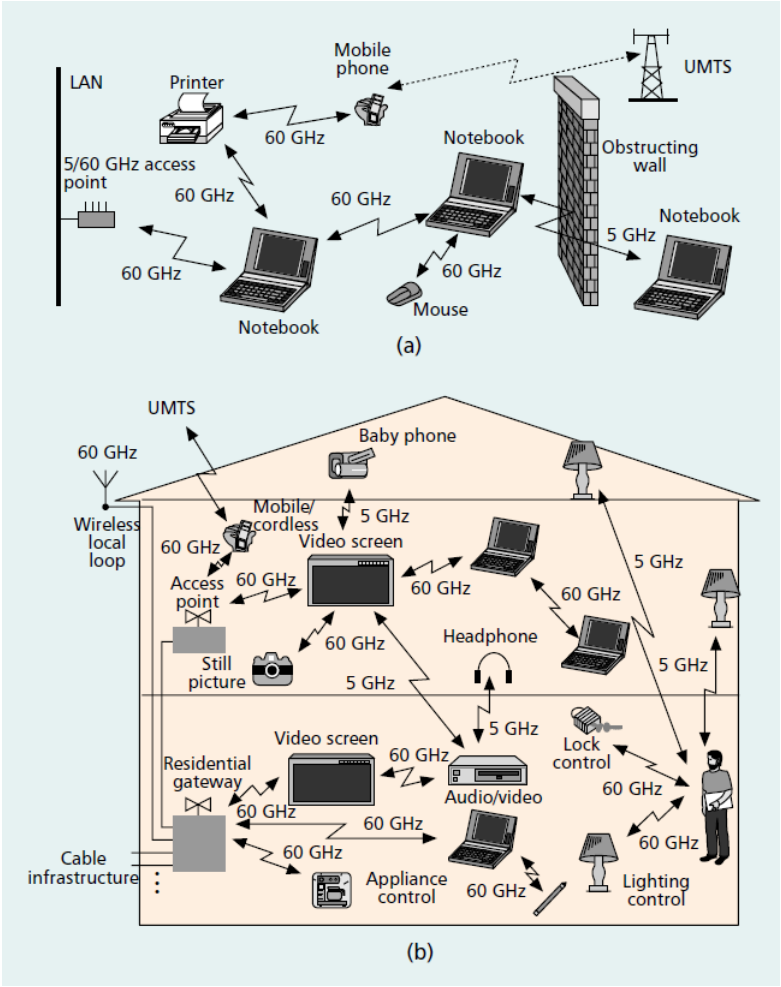


Figure 1-2: Scenario for dual band wireless system in (a) office or (b) home environment [2].

One attractive feature for mm-wave frequencies is their short wavelengths, which translates to a dramatic size reduction in RF components. As a result, miniaturized RF front-ends with on-chip antennas for integrated beam-steering would be realizable. The small wavelength makes it feasible to employ a large number of antenna elements and provide highly directional beams which can mitigate the propagation loss issue. Moreover, theoretical studies in recent years have acknowledged that the mm-wave is a promising candidate to fulfill the requirements of the next generation (5G) cellular system communication.

1.1.2 Reconfigurable RF-MEMS components

RF switches are reconfigurable components acting as principal elements of any RF circuit. They need to be there to switch between transmit and receive lines in a transceiver, to select among multiple antennas, or to rout the RF signal to a certain block in a multiband system or phase shifter. Switches are usually located immediately next to the antennas in either the receiving or transmitting paths of a communication system. RF MEMS switches are basically miniaturized versions of mechanical relays. Although there are a few constraints hindering the widespread use of MEMS switches in competition with classic semiconductor types (PIN diodes, GaAs MESFET or JFET-based switches), such as lower power handling and speed, higher required voltage level and less reliability in terms of duty cycles, they would still stand out for their performance in terms of insertion loss, isolation, linearity and power consumption in comparison with semiconductor counterparts, especially at the mm-wave region. Table 1.1 shows a comparison between competing systems.

Other important reconfigurable elements in RF circuits are phase shifters, which are the fundamental components for phased array antennas required for beam-steering. Phased array antennas are in demand for mm wave, particularly for the 60 GHz band, to counteract severe direction-dependent path loss and shadowing effect. MEMS phase shifters exploiting RF switches or tunable (switchable) capacitors help to reduce insertion loss, the number of amplifiers needed in the circuit, and power consumption. On the one hand, traditional nonreciprocal toroidal ferrite phase shifters are too bulky and costly for many applications, while on the other, current solid state phase shifters based on PIN diodes or FET transistors are too lossy. Table 1.2 compares losses of RF MEMS and GaAs FET phase shifters. As can be seen, the difference is significant for mm-wave bands.

Tunable filters are the other essential reconfigurable passive RF blocks in transceiver circuits. At a cellphone front-end, for instance, dozens of fixed filters might be required for a wide channel covering. A

reliable tunability mechanism can shrink transceiver size by combining multiple filters into one. A tuning element is mostly a variable capacitor. Solid state tuning elements are vulnerable to noise and high input power due to their nonlinearity. Some imperative requirements for a good tuner are high Q (small resistance), low power consumption, linearity and compactness, all of which can be satisfied by RF-MEMS devices. Table 1.3 presents a comparison between RF-MEMS tuners and their counterparts.

Table 1-1: Comparison between RF-MEMS switches and their PIN/FET counterparts [3].

Parameter	RF MEMS	PIN	FET
Voltage (V)	20–80	±3–5	3–5
Current (mA)	0	3–20	0
Power consumption[a] (mW)	0.05–0.1	5–100	0.05–0.1
Switching time	1–300 μs	1–100 ns	1–100 ns
C_{up} (series) (fF)	1–6	40–80	70–140
R_s (series) (Ω)	0.5–2	2–4	4–6
Capacitance ratio[b]	40–500[b]	10	n/a
Cutoff frequency (THz)	20–80	1–4	0.5–2
Isolation (1–10 GHz)	Very high	High	Medium
Isolation (10–40 GHz)	Very high	Medium	Low
Isolation (60–100 GHz)	High	Medium	None
Loss (1–100 GHz) (dB)	0.05–0.2	0.3–1.2	0.4–2.5
Power handling (W)	<1	<10	<10
Third-order intercept point (dBm)	+66–80	+27–45	+27–45

[a] Includes voltage upconverter or drive circuitry.

[b] Capacitive switch only. A ratio of 500 is achieved with high-ε_r dielectrics.

Table 1-2: Comparison between average losses of MEMS and GaAs FET 3-bit phase shifters [4].

Freq. (GHz)	Loss RF MEMS (dB)	Loss GaAs FET (dB)
X-band (10)	-0.9 to -1.0	-3 to -4
Ka-band (35)	-1.7 to -2.0	-6 to -7
V-band (60)	-2.3 to -2.6	-8 to -9
W-band (94)	-2.6 to -3.0	-9 to -10

Table 1-3: Comparison between different tuning methods [5].

	YIG	BST	Schottky Diode	p-i-n Diode	MEMS
Q	500–2,000	30–150	30–150	R_s = 1 Ω	50–400[a]
Tuning Range	2–18 GHz	C_r = 2–3	C_r = 3–5	High	C_r = 2–100[c]
Tuning Speed	ms	ns	ns	ns	μs[d]
Linearity, IIP3 (dBm)[e]	≈20	10–35[b]	10–35[b]	>33	>60
Power Handling (mW)[e]	50–200	20–200	10–100	High	100–1,000
Power Consumption	0.5–5 W	0	0	20–30 mA	0
Temperature Sensitivity	High	High	Low	Low	Low
Biasing	Magnet	High R	High R	LC choke	High R
Planar	No	Yes	Yes	Yes	Yes
Cost	High	Low	Low	Low	Low[f]

- PIN diode used as a switched capacitor tuner (R_s = 1 Ω), 20–30 mA/diode.
- *Q* values given for 0.1–10 GHz applications for all devices except MEMS.
- Linearity and power handling for band-pass filter: two-pole, 3–5% bandwidth.

a) *Q* applicable for 0.1–100 GHz.
b) Large values can obtained as 1 × 3 arrays or anti-series diode pairs.
c) MEMS used an analog varactor or switched capacitor.
d) Miniature MEMS can be switched at 200–800 ns.
e) Power handling and linearity are in tunable networks (filters) and not in 50 Ω environments.
f) Potential for low cost in high volume applications.

1.1.3 CMOS-MEMS integration

Silicon-based CMOS (Complementary Metal-Oxide-Semiconductor) technology is one of the most reliable IC fabrication methods, having a mature process and high integration with other analog/digital circuits. CMOS is therefore desirable for the implementation of communication circuits. Advanced CMOS processes based on Silicon-on-insulator (SOI) technology with multiple metallization layers and minimum gate lengths of a few tens of nanometers are required to fabricate microprocessors with millions of transistors on a single chip. Even technologies from 20 years ago are sufficient for most transducer elements and microsystem applications [6]. However, advances in CMOS technology, together with knowledge of RF circuit design, could make it possible to implement all fundamental RF components and create a fully integrated transceiver on CMOS [7].

To make hardware-sharing between a growing number of different wireless standards possible, the development of multiband systems with tunable components is required. Reconfigurable MEMS components integrated on CMOS with the potential to be electronically controlled offer a linear and miniaturized solution. Even the problem of high actuation voltage needed for electrostatic MEMS switches can be offset by means of charge pumps in a monolithically integrated CMOS-MEMS circuit. If monolithic integration on CMOS is realized, phase shifters and power amplifiers would come together on a single chip, leading to an even greater reduction in size as well as number of circuit elements. It is important to find an integration solution for these MEMS structures and Silicon-based CMOS components. The CMOS-MEMS mm-wave circuit components proposed in the literature have not met the satisfying performance level required for existing applications. The ultimate goal would be to realize a full radio frequency system on chip (RF-SoC) functioning in the mm wave range and having reconfigurable RF MEMS structures integrated on CMOS.

1.2 Objective

The objective of this research is to design and fabricate low loss and high isolation miniaturized RF-MEMS reconfigurable devices operating at the mm-wave region (60 GHz and 77 GHz bands in particular) and monolithically integrated on CMOS chips by means of back-end-of-line (BEOL) post-processing methods. The focus of this thesis is CMOS-MEMS capacitive SPST and SPNT switches and switched capacitors, which can be employed to realize more complicated designs such as multi-port switches and switch matrices.

1.3 Thesis Outline

- Chapter 2 presents a literature review. Pioneers and research groups working in the field of CMOS-MEMS integration by means of BEOL post-processing are introduced. The chapter also summarizes previous works which reported on passive RF-MEMS components (inductors, tunable capacitors, switches, phase shifters and tunable filters) integrated on CMOS using the above method.
- Chapter 3 introduces CMOS 0.35 μm BEOL layers and the proposed post-processing steps to create MEMS structures out of the layers. A mechanical analysis of residual stress and post-release deflection of MEMS structures fabricated by this method is also presented.
- In Chapter 4, mm-wave reconfigurable MEMS devices, including SPSP and SP3T switches and a DMTL component to be integrated on CMOS 0.35 μm by means of post-CMOS fabrication, are presented. As well, design strategies and RF simulation results are reported.
- Chapter 5 provides details on fabrication methodology and optimized post-processing recipes. SEM pictures of the successfully fabricated CMOS-MEMS devices are provided.
- Chapter 6 concludes the thesis by giving a summary, addressing the existing challenges, and presenting potential applications and future work.

Chapter 2

Literature Review

2.1 CMOS-MEMS integration methods and pioneers

Advances in semiconductor technology over the past few decades have paved the way for the monolithic integration of MEMS structures with CMOS electronics [6, 8, 9]. For many of the available products on the market, hybrid integration techniques (rather than monolithic) such as chip-to-wafer bonding or wafer-to-wafer bonding techniques have been used. The advantage of the hybrid method is that development time is short and it is possible to independently optimize CMOS and MEMS processes. However, assembly is still rather costly and interconnections add parasitic noise and interference [10].

Monolithic integration, on the other hand, helps with miniaturization of the chips and reduces manufacturing costs in large-scale production. Moreover, a system having electronic components in close vicinity to MEMS structures with no need for extra interconnecting circuitry would have a better signal-to-noise ratio. This type of integration is possible by using several different methods, depending on at which level the MEMS fabrication process is taking place, before, during or after CMOS fabrication. The first three approaches are referred to as pre-CMOS, intra-CMOS and post-CMOS, respectively. The fourth alternative method, which is the one we focus on here, is post-processing the CMOS back-end-of-line (BEOL) layers of an already fabricated CMOS chip by means of several dry and wet etching steps to release some MEMS structures.

This method enables monolithic integration with no need for extra film deposition or to interfere with routine CMOS fabrication process. Furthermore, unlike other methods or integration by means of flip chip bonding, this approach requires no additional lithography for patterning. However, the main disadvantage is that the MEMS structures to be realized are restricted by the material type, number, thickness and minimum feature size of BEOL metal layers available for each CMOS process. Table 2.1 shows a comparison between the different monolithic integration methods mentioned above.

Table 2-1: Comparison of CMOS-MEMS integration methods [11].

	Pre-CMOS	Intra-CMOS	Post-CMOS	Postprocessing of CMOS-BEOL Layers
Interruption of the CMOS process	No	Yes	No	No
Thermal budget limitation on MEMS	No	Yes	Yes	No
Limitations on selecting MEMS layer thicknesses	No	No	Yes	Yes
Effective use of CMOS area	Yes	No	Yes	No
Possible control of residual stress of MEMS layers	Yes	Yes	No	No
Need for planarization steps	Yes	No	Yes	No
Foundry requirements	Possible by separate CMOS and MEMS foundries	Possible only by using a dedicated one foundry for both CMOS and MEMS.	Possible by separate CMOS and MEMS foundries	Possible by CMOS foundry and a clean with basic dry and wet etching capabilities
Integration development efforts	Medium	High	Medium	Low
Additional mask requirements	Yes	Yes	Yes	No (A mask-less process)
Integration level	Wafer level	Wafer level	Wafer lever	Chip level or wafer level

The fourth aforementioned approach was introduced at the University of Alberta, Canada [12], and has since spawned several groups worldwide working in the field. The group headed by professor Gary Fedder of Carnegie Mellon University (in Pennsylvania, USA) developed a mask-less post-processing capable of creating high-aspect-ratio metal-dielectric stack structures from BEOL metals by means of a sequence of several dry etching steps, for which the very top metal layer is used as a protective mask [13, 14], as shown in Figure 2.1. The process is commercially known as ASIMPS (Application Specific Integrated MEMS Process Services) and is implemented using several CMOS technologies with Aluminum or Copper BEOL metal layers. Over the past two decades, researchers have been active in the field, applying the proposed process to fabricate integrated CMOS-MEMS accelerometers [15-18], gyroscopes [19], micro-mirrors [20], mechanical resonators [21], and various RF circuit components [22-27].

Professor Weileun Fang and his team from the National Tsing Hua University in Taiwan are also pioneers in the field. They have published several reports on CMOS-MEMS accelerometers [28-32], capacitive sensors [33-35], and mechanical resonators [36-40]. The ASIMPS process used by Garry Fedder's group

created structures with metal layers laminated and enclosed by oxide, restricting the out-of-plane movement and vertical actuation. Fang et al. came up with a revised post-processing method which used the solution of H_2SO_4 / H_2O_2 to etch through exposed metal layers and Tungsten vias to create a micro air gap, as shown in Figure 2.2. The method was used for an out-of-plane accelerometer design [41].

Professor Raafat Mansour's group at the Center for Integrated RF Engineering (CIRFE), University of Waterloo, has also been actively researching the field of CMOS-MEMS integration by means of BEOL post-processing. They reported the fabrication of CMOS-MEMS scanning microwave microscopy (SMM) systems [42], scanning probe microscopes (SPMs) [43], and atomic force microscopes (AFMs) [44, 45], as well as numerous CMOS-MEMS RF circuit components [46-51]. To confront the limitations imposed by the ASIMPS post-processing method, a modified process was presented by CIRFE members which had a few extra steps. A wet etching recipe was used to remove sacrificial metal layers and create suspended MEMS components on top of the metals. As well, a second RIE step for the top oxide was suggested to increase the upward curvature of the released structures for certain applications [47]. The proposed post-processing steps are shown in Figure 2.3.

Another active research group studying CMOS-MEMS RF devices are from the National Chung Cheng University, Taiwan. By means of CMOS post-processing, Chia-Chan Chang et al. demonstrated dual-state and multi-state electrostatic fishbone-beam-drive actuators in [52] (as shown in Figure 2.4), which were developed and modified further in [53]. The actuators have since been applied in all sorts of reconfigurable RF front-end components mostly operating in V/W band frequencies, such as slot antennas [52, 53], filters [52-54] and phase shifters [55].

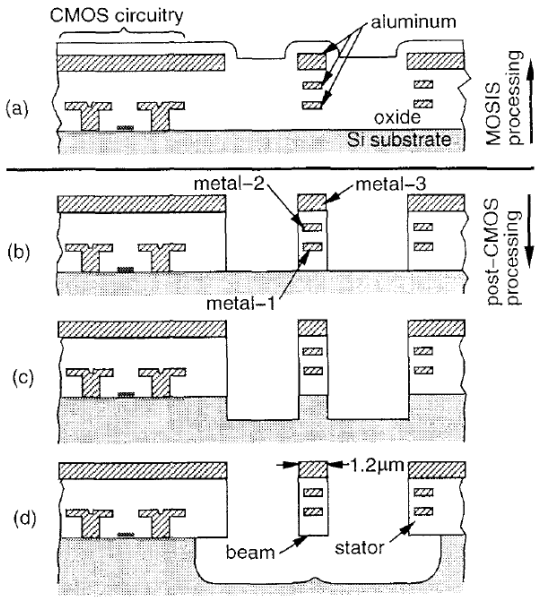


Figure 2-1: The process flow suggested by Garry K. Fedder's group from Carnegie Mellon University for fabrication of high-aspect-ratio microstructures (on a 3-metal CMOS process offered by MOSIS): (a) the CMOS dice from foundry, (b) after anisotropic dry etch of oxide, (c) after anisotropic dry etch of exposed substrate, and (d) after isotropic dry etch of Si to release the structures [13].

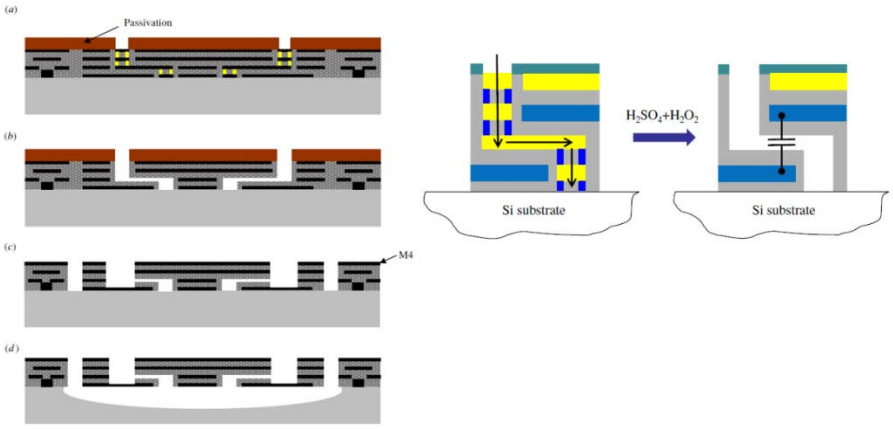


Figure 2-2: The steps suggested by Weileun Fang's group for the 4-metal CMOS 0.35 μm BEOL post-processing: (a) as-received chip (Tungsten vias between metal layers are shown in yellow), (b) after wet etching of the exposed metal layers and vias to create the air gap, (c) after RIE of oxide, and (d) after isotropic etch of substrate to release the structure [41].

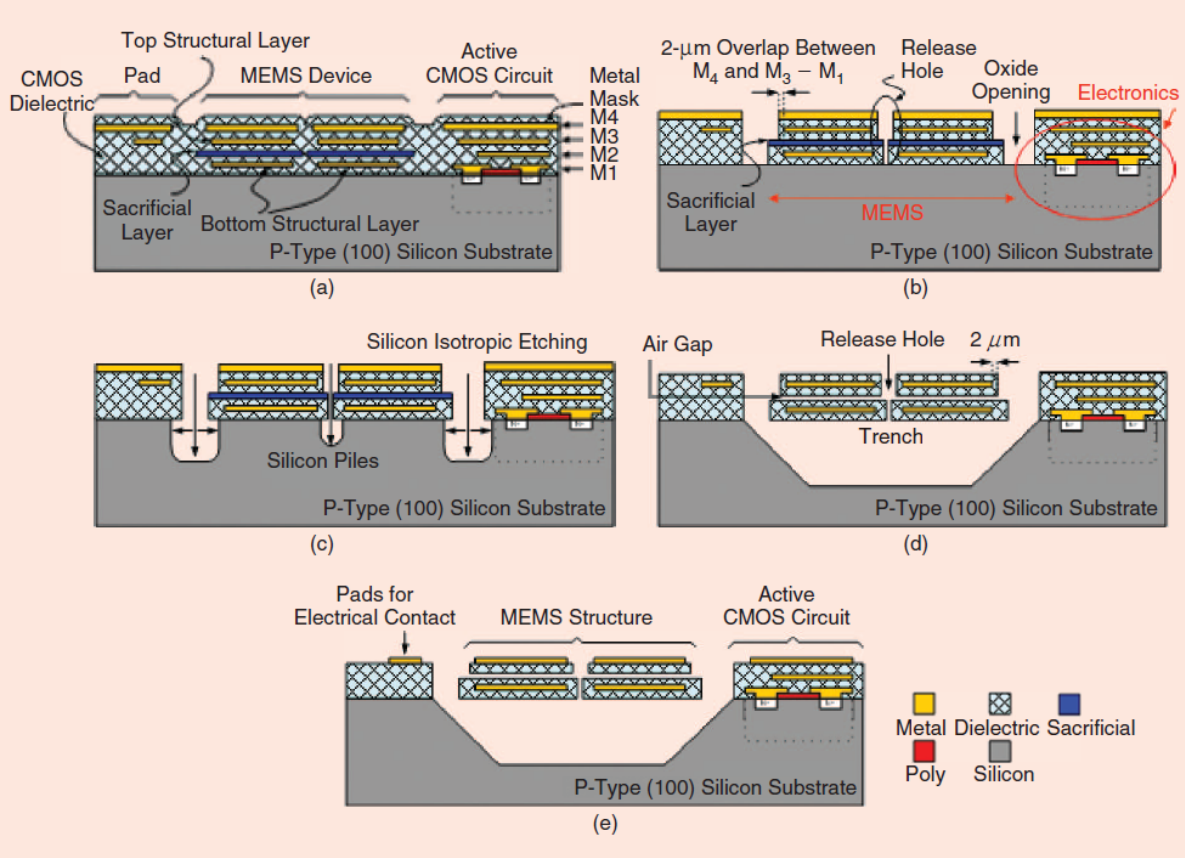


Figure 2-3: The post-processing steps of CMOS 0.35 μm BEOL layers offered by the CIRFE group at the University of Waterloo: (a) as-received chip from the foundry, (b) after the first oxide RIE, (c) after the silicon RIE, (d) after wet etching of the sacrificial metal layer and anisotropic wet etch of Silicon, and (e) after the second RIE of oxide [11].

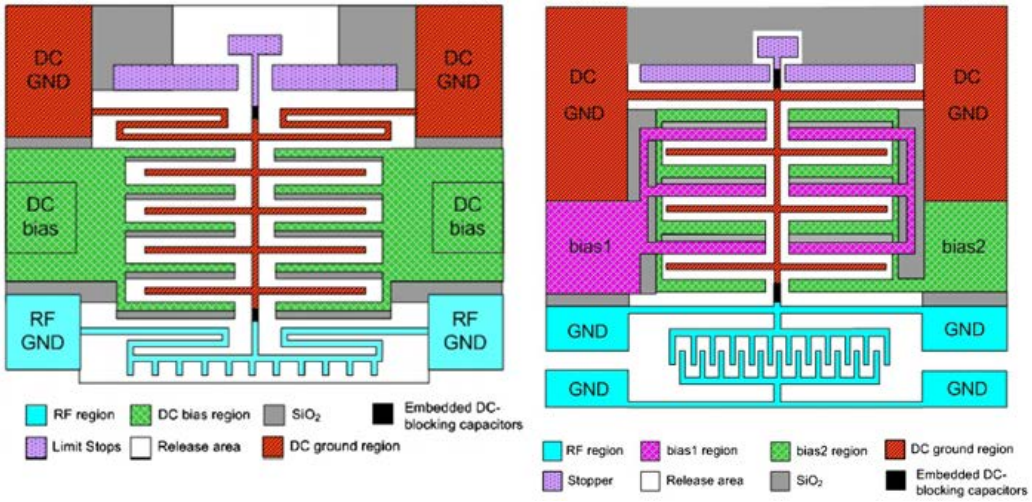


Figure 2-4: The dual-state (left) and multi-state (right) fishbone-beam-drive actuators used in reconfigurable CMOS-MEMS devices proposed by Chia-Chan Chang et al. [52].

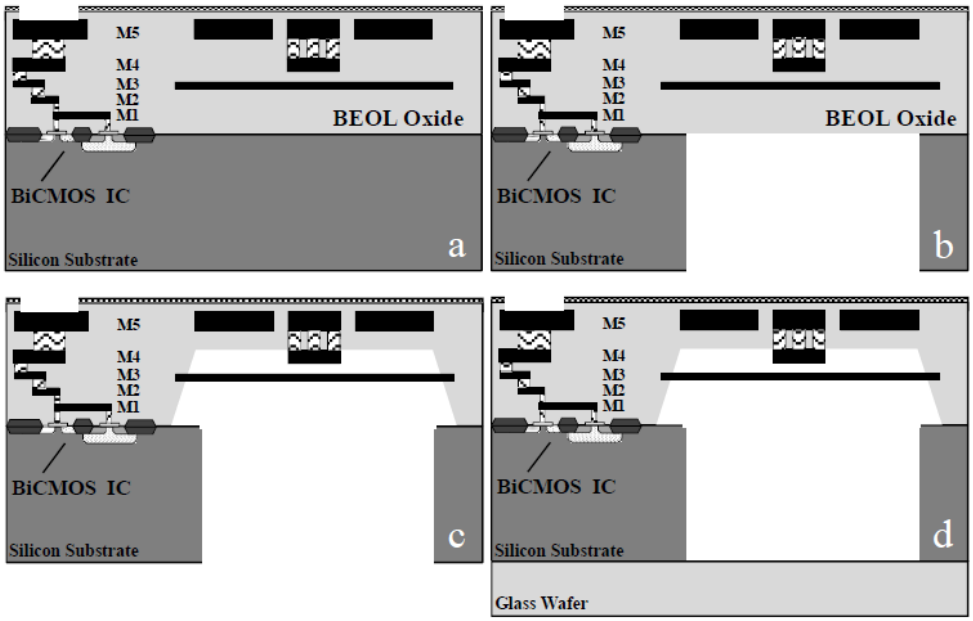


Figure 2-5: Post-processing steps proposed for IHP's 0.25 μm SiGe BICMOS BEOL: (a) chip from the foundry, (b) after back-side Silicon etch, (c) after wet etch of BEOL oxide, and (d) after packaging [57].

It is possible to apply similar post-processing methods to BiCMOS technology and benefit from the higher voltage value available. The IHP microelectronics group from Germany [56-58] proposed a post-processing method to be used for 0.25 μm SiGe BICMOS BEOL, which consisted of deep back-side

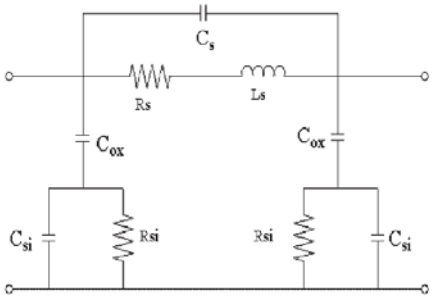
etching of Silicon substrate, wet etching of BEOL oxide to release MEMS structures, and finally a wafer level packaging step by bonding glass substrate to the back, as shown in Figure 2.5.

Dr. Ching Liang Dai from National Chung Hsing University in Taiwan is another pioneer in this research area and has published numerous works on BEOL CMOS-MEMS mechanical resonators [59, 60], sensors [61], micromirrors [62], and several RF devices, including switches [7, 63-66] and tunable capacitors [67-69]. Some of his works are presented in section 2.2.

2.2 CMOS-MEMS RF devices implemented by BEOL post-processing method

2.2.1 Inductors

Micro-inductors are necessary components of RF-MEMS circuits being used in LC tanks, voltage-controlled oscillators (VCOs), and DC convertors. The figure of merit of an RF inductor is its quality factor, which demonstrates the capacity of the inductor to store energy. Based on the equivalent circuit model of the on-chip inductor shown in Figure 2.6, improving the quality factor is possible by reducing the series resistance (i.e., by using highly conductive metals and increasing the line's cross-section to defeat the skin effect) and eliminating substrate losses by blocking the signal path to the low-resistivity CMOS substrate. It is also important to increase the self-resonant frequency of the inductor beyond the operating frequency.



$$Q = \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + [(\omega L_s/R_s)^2 + 1]R_s} \cdot \left[1 - \frac{R_s^2(C_s + C_p)}{L_s} - \omega^2 L_s(C_s + C_p)\right]$$

$$= \frac{\omega L_s}{R_s} \cdot \left(\begin{array}{c}\text{Substrate loss}\\ \text{factor}\end{array}\right) \cdot \left(\begin{array}{c}\text{Self-resonance}\\ \text{factor}\end{array}\right)$$

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{Si}} + \frac{R_{Si}(C_{ox} + C_{Si})^2}{C_{ox}^2}$$

$$C_p = C_{ox} \cdot \frac{1 + \omega^2(C_{ox} + C_{Si})C_{Si}R_{Si}^2}{1 + \omega^2(C_{ox} + C_{Si})^2 R_{Si}^2}$$

Figure 2-6: Equivalent circuit model of on-chip inductor and calculation of its quality factor [67].

Meander or spiral inductors can be easily made on CMOS with a stack of BEOL metal layers. To suppress substrate losses, it is necessary to micro-machine the lossy silicon substrate beneath the inductor lines. Also, a post-processing step of etching inter-turn oxide walls helps increase the self-resonant frequency [22]. Due to the lower resistivity and skin depth of the material, Copper inductors are preferred to Aluminum ones.

Both types of inductors in the order of a few nH were realized on CMOS 0.18μm [22, 70] and 0.35μm [67, 71], respectively.

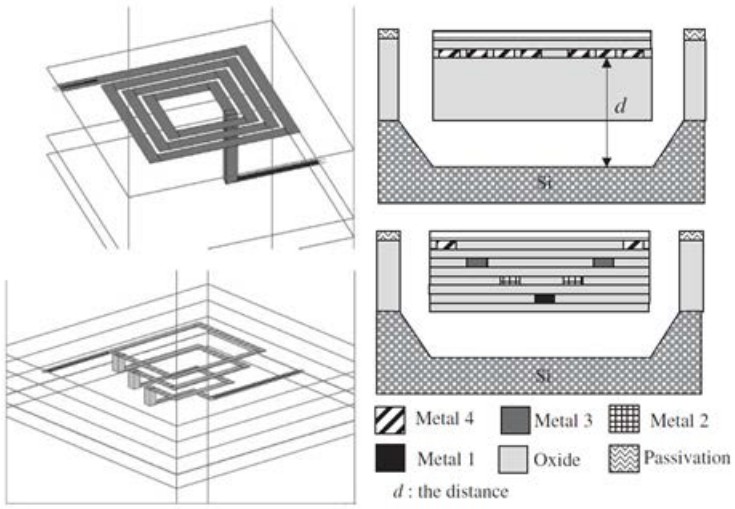


Figure 2-7: Fabrication of planar spiral (top) and conical spiral (bottom) inductors on CMOS 0.35 μm with quality factor of around 4 working at around 4 GHz [67].

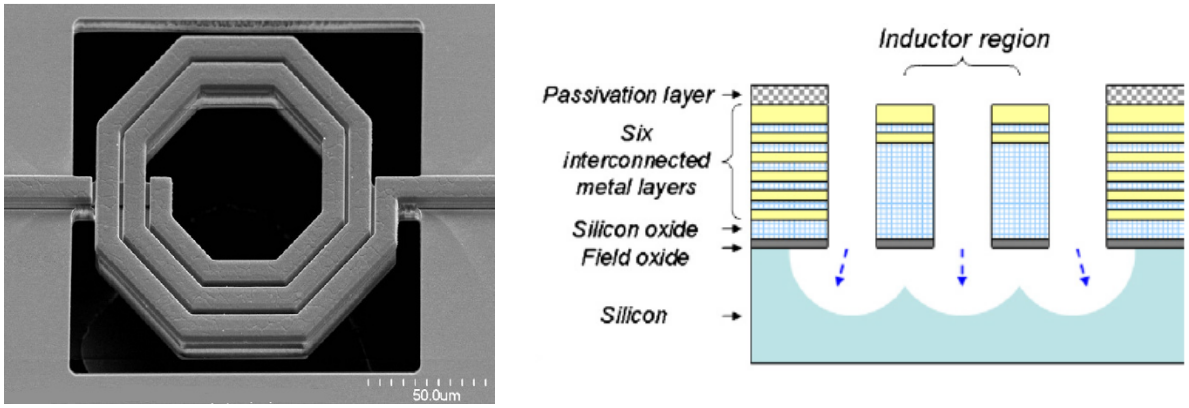


Figure 2-8: SEM picture (left) and schematic (right) of a CMOS MEMS spiral inductor implemented on CMOS 0.18 μm. The inductor is 1.88 nH at 8.5 GHz with a quality factor up to 15 [70].

2.2.2 Tunable capacitors

Variable MEMS capacitors have application in VCOs, reconfigurable RF devices such as filters, phase shifters and impedance matching networks. Tuning a MEMS capacitor is possible in a configuration where electrodes can be moved with respect to each other by means of actuators either electrostatically or electrothermally. Polysilicon layers available in CMOS BEOL can be used as heaters for electrothermal actuation, which has the benefit of linear tuning and lower required actuation voltage compared to electrostatic actuation. However, the consumed DC power is higher. Two important design features for tunable capacitors that need to be maximized are the tuning ratio (which is the ratio between capacitor values at two extreme states) and capacitance density per unit area of the chip. Tunable capacitors fall into two categories: lateral interdigital and vertical parallel plates.

An electrostatically actuated MEMS parallel plate capacitor offers a higher capacitance density per unit area, higher self-resonant frequency, lower parasitic inductance (and therefore better quality), and zero DC power consumption. A design consisting of 100 small tunable micro-capacitors in parallel was implemented on CMOS 0.35 μm by Dai et al. [67]. Each cell consisted of two fixed plates (made from the Polysilicon layer and M_4 top metal layer) and one movable plate suspended by supporting beams (made from M_2 layer) in the middle, which were forced to move up or down by applied voltage values at two sides. During the post-processing, the M_1 and M_3 BEOL metal layers were sacrificed to create air gaps. A capacitance variation of 0.05 pF was reported for 40 V bias voltage at 30 MHz frequency.

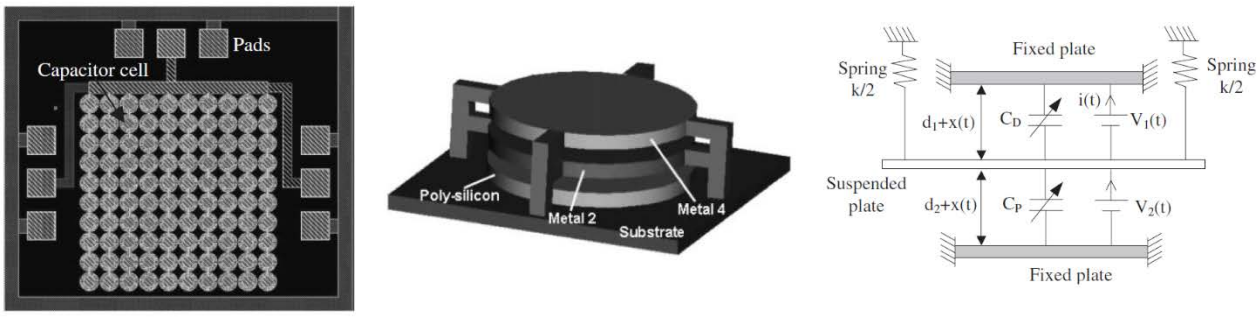


Figure 2-9: CMOS-MEMS tunable capacitor cells implemented on CMOS 0.35 μm [67].

The CIRFE group also demonstrated parallel plate capacitor designs using TSMC 0.35 μm CMOS technology [47]. The substrate etching step to create an air trench under the capacitor structure helped increasing the quality factor and self-resonant frequency. A tristate capacitor was made using two plates on

M_1 and M_3, suspended over an air trench inside the substrate, and anchored on two sides by eight supporting beams which also functioned as RF signal routes. The air gap between the two plates was made by wet etching a sacrificial M_2 metal layer. The intentional curling of the plates due to post-release residual stress helped increasing the capacitance ratio. The reported tuning range was 460% at 1n Ghz. They also presented another structure (not shown here) with more supporting beams to suppress excessive curling of the plates, resulting in a continuous tunable capacitor with no pull-in, a tuning range of 115%, and a quality factor of better than 300 at 1.5 GHz.

G. Fedder's group reported the design and fabrication of several interdigitated tunable capacitors using their post-processing methodology [23, 25, 26]. In [26], they proposed a 3-bit interdigital tunable capacitor on a 0.35 μm BICMOS chip, using a configuration consisting of several MEMS switched parallel capacitors, for which both out-of-plane (vertical) electrothermal and in-plane (lateral) electrostatic actuations were used to change the capacitance value. The tuning ratio and capacitance density were optimized in their proposed configuration and actuation scheme, as shown in Figure 2.11. The reported tuning ratio and quality factor (at 1 GHz) were 60 and 150, respectively.

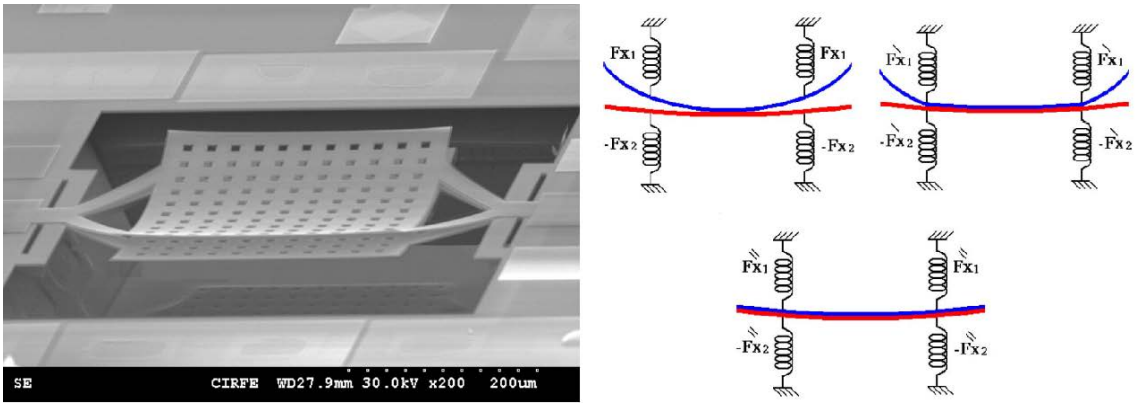


Figure 2-10: Tristate parallel plate variable capacitor fabricated on CMOS 0.35 μm, SEM picture (left) and schematic diagram of the three possible states (right), before collapse, at the first and second collapse points are shown [47].

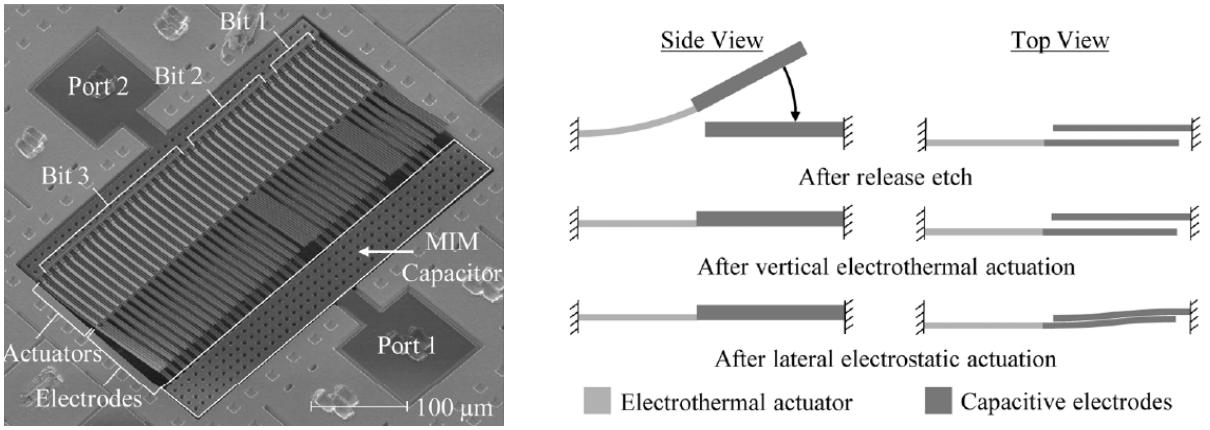


Figure 2-11: CMOS-MEMS 3-bit tunable interdigital capacitor with electrothermal and electrostatic actuation mechanisms [26].

2.2.3 Switches

Among the earliest works was one reported by Chiang Liang Dai [63]. It involved a CPW switch using a pair of electrostatic parallelogram actuators implemented on a 0.6 μm 3-metal single polysilicon CMOS chip by a mask-less post-processing method. Two T-type connecters controlled by actuators were moved towards the CPW signal line to turn the switch OFF. The operating frequency was in the range of 10-20 GHz, with insertion loss and isolation reported to be 6.8 dB and 7.8 dB, respectively.

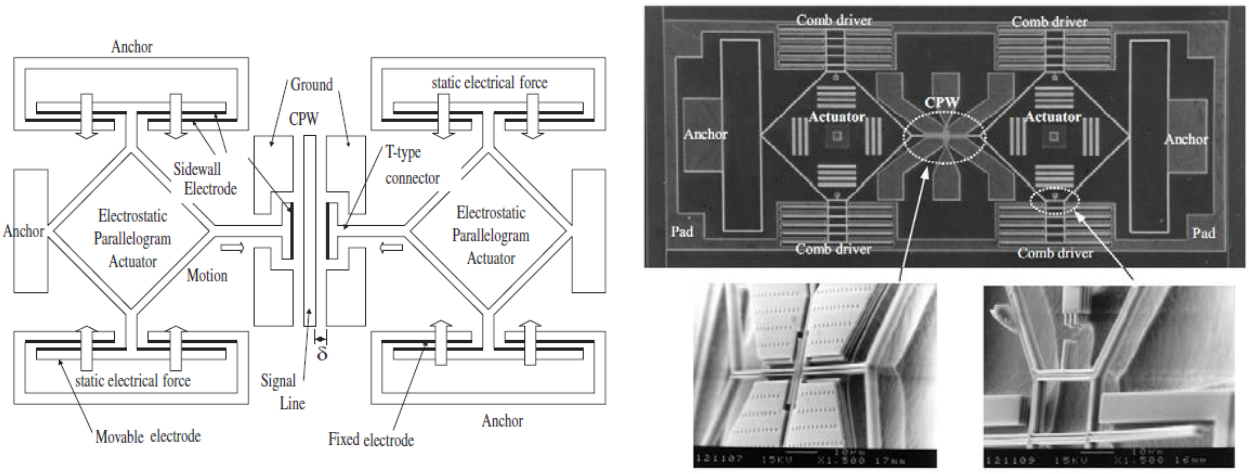


Figure 2-12: Schematic (left) and SEM picture of the CMOS-MEMS switch chip with electrostatic parallelogram actuators implemented on 0.6 μm CMOS chip [63].

Dai et al. also proposed some high performance switches. Several CPW capacitive switches with suspended membranes and supporting springs on CMOS 0.35 μm, for which only a single step of wet etching of sacrificial dielectric material was needed as post-processing, were reported in [7, 64-66]. The required DC voltage for electrostatic actuation of their designed switches was relatively low (less than 20 V for all cases and as small as 7 V for the one reported in [65]). Figure 2.13 shows a schematic and picture of the switch in [66] operating with 2 dB insertion loss and 15 dB of OFF-state isolation at 50 GHz.

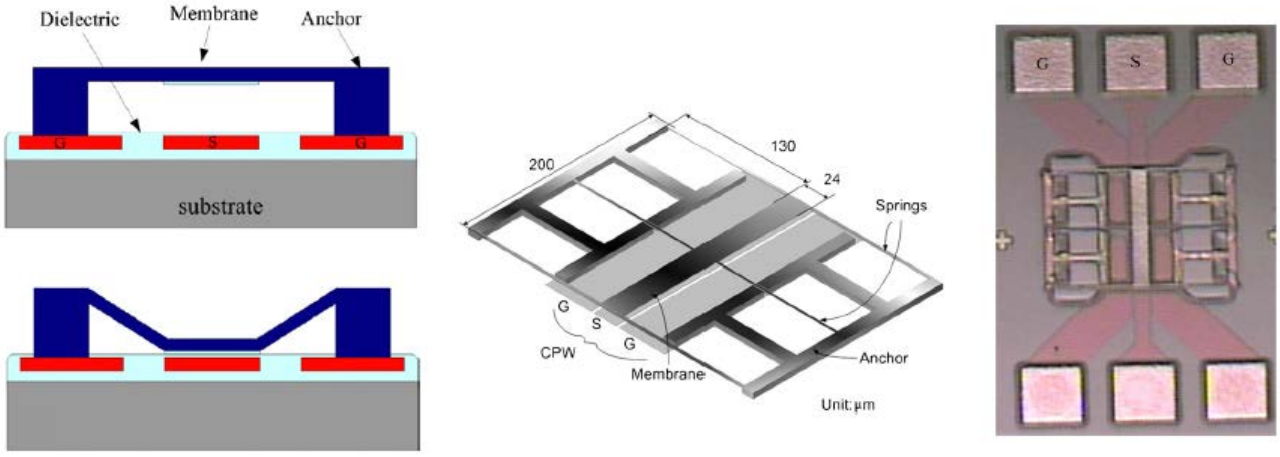


Figure 2-13: Schematic and photograph of the capacitive CPW switch with suspended membrane and supporting springs fabricated on CMOS 0.35 μm [66].

Using the back-side processing method described earlier (see Figure 2.5), M. Kaynak et al. fabricated mm-wave RF-MEMS switches integrated with IHP 0.25 μm SiGe BICMOS technology [56-58]. Figure 2.14 shows a designed capacitive switch in [56], where a grounded membrane on M_3 layer would be electrostatically actuated. The switch had a capacitance ratio of 10 and operated from 60 GHz to 110 GHz, with insertion loss and isolation exceeding 1.65 dB and 15 dB, respectively. Reliability tests proved consistent performance after ten billion switching cycles.

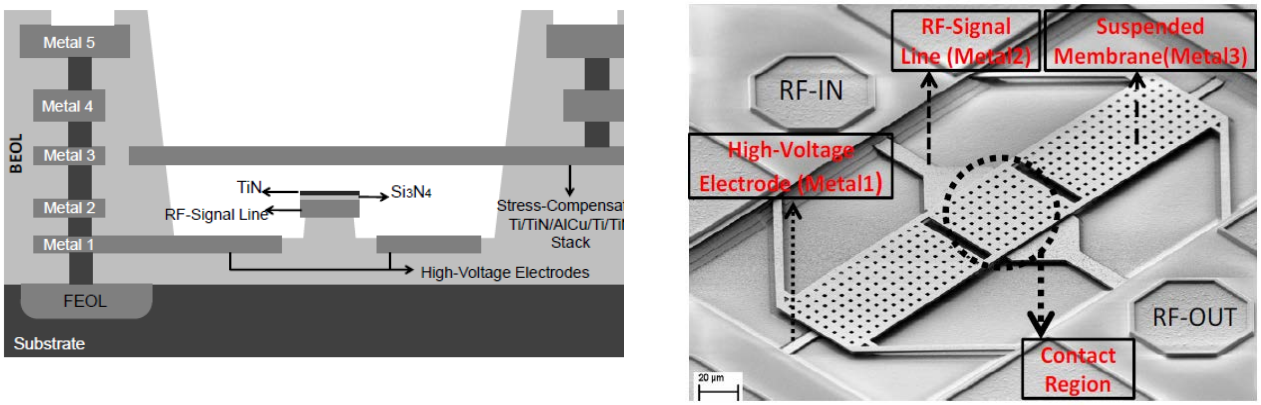


Figure 2-14: Cross section view (left) and SEM picture of mm-wave capacitive RF MEMS switch integrated with IHP 0.25 μm SiGe BICMOS technology [56].

Capacitive shunt switches were implemented on TSMC CMOS 0.35 μm by the CIRFE group [49]. Two curled-up plates suspended over the ground conductor were actuated by electrostatic force from a pair of actuation electrodes located inside the CPW gap. For a complete collapse of the plates, an extra DC voltage had to be applied between the CPW signal and ground lines (the required voltage values applied to the electrode and CPW ground were 82 V and 25 V, respectively). The stress-induced warpage helped increasing the capacitance ratio to 91:1. The reported insertion loss and isolation were better than 1.4 dB and 19dB from 10 GHz to 20 GHz.

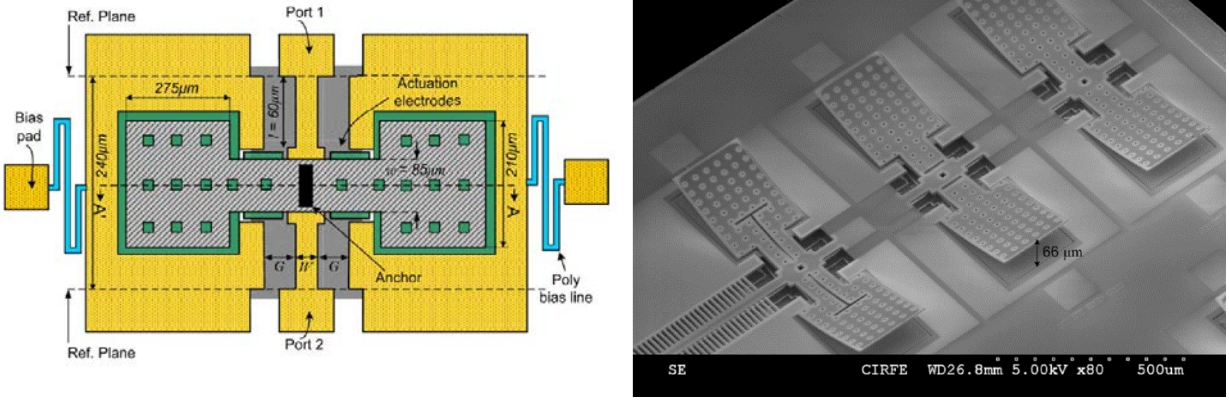


Figure 2-15: Schematic and SEM picture of fabricated electrostatically actuated shunt capacitive switch on CMOS 0.35 μm [49].

2.2.4 Phase shifters

Garry Fedder's group developed their previously reported [26] CMOS-MEMS digital capacitor integrated on 0.35 μm BiCMOS chip with both electrothermal and electrostatic controlling mechanisms to load a micromachined transmission line and construct a distributed MEMS phase shifter [27]. The operation frequency was 32 GHz and the phase could be adjusted to 16 digital values (4 bit), with a maximum range exceeding 300°. The measured insertion loss was around 2.9 dB.

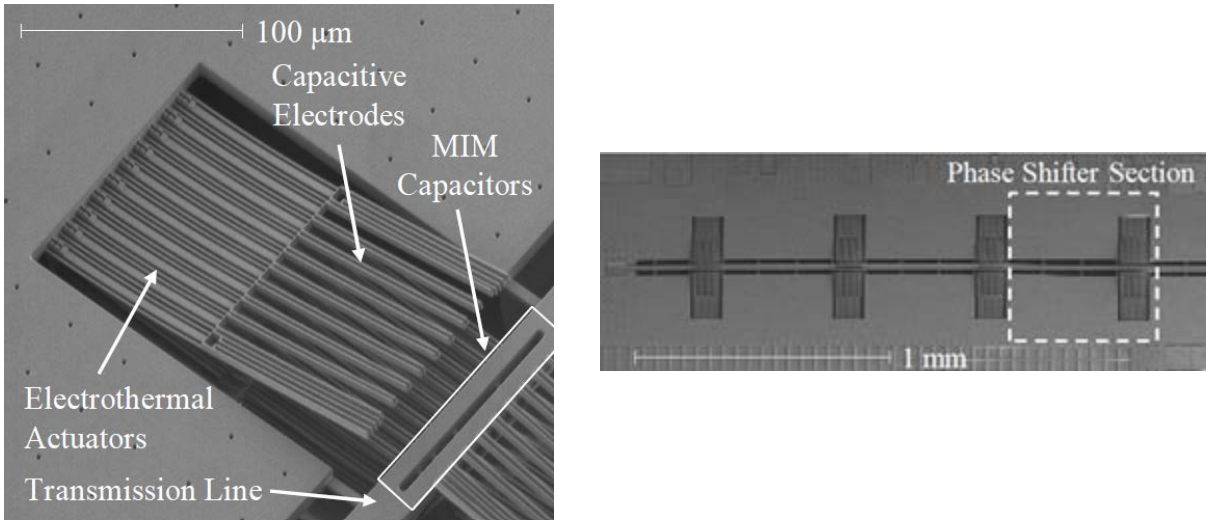


Figure 2-16: Digital capacitor (left) as a tuning component in a distributed MEMS phase shifter (right) integrated with BiCMOS 0.35 μm technology [27].

Chia Chan Chang et al. applied their dual-state bi-directional fishbone actuator [52] to act as an interdigitated variable capacitor and designed a V-band reflection type phase shifter using a broadside coupler implemented on BEOL of CMOS 0.18 μm [55]. The coupler structure is shown in Figure 2.17. The measured insertion loss was 2.2±1 dB from 55 GHz to 65 GHz and three states of phase were achieved with actuation voltage below 46 V.

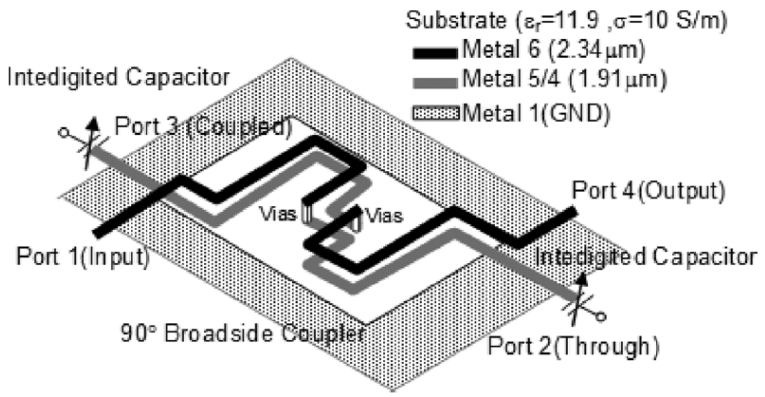


Figure 2-17: Schematic of reflection type phase shifter made on CMOS 0.18 μm BEOL layers [55].

2.2.5 Tunable filters

S. Fouladi et al. from the CIRFE group demonstrated a 2-pole coupled line tunable bandpass filter integrated on CMOS 0.35 μm. The tuning elements were parallel plate variable capacitors made by BEOL post-processing, similar to the ones reported in [47]. Centre frequency, relative bandwidth, tuning range, and insertion loss of the tunable filter were reported to be 9.5 GHz, 9 %, 17 % and 5.6 dB, respectively.

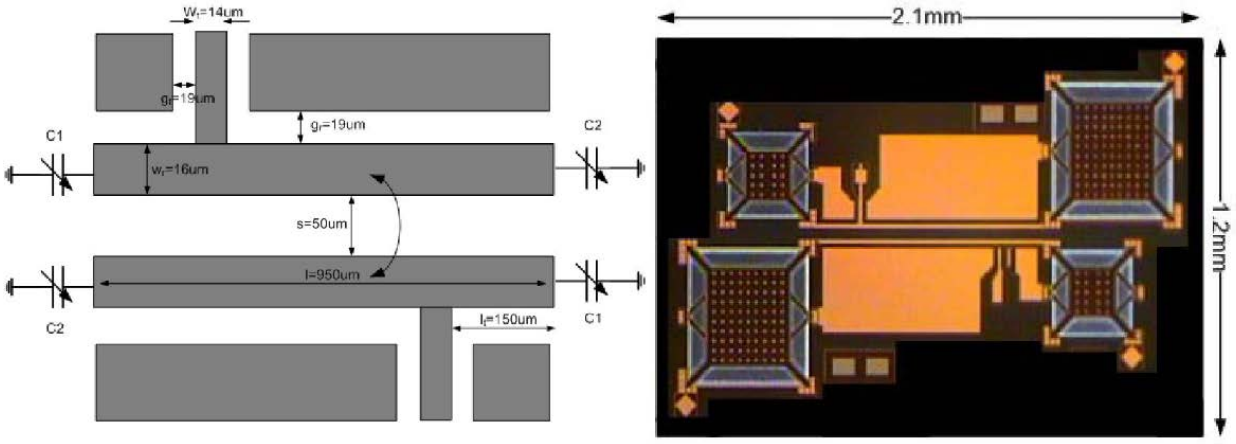


Figure 2-18: Tunable coupled line band pass filter demonstrated on CMOS 0.35 μm with MEMS parallel plate variable capacitors as tuning elements [46].

The Taiwanese group of Professor Chia-Chan Chang designed an mm-wave reconfigurable band stop filter on CMOS 0.35 μm [54], where the stop-band was switched by the fishbone actuator which could

adjust the open-stub capacitance. Tuning the resonance frequency between 50 GHz to 60 GHz with isolation better than 35 dB was reported.

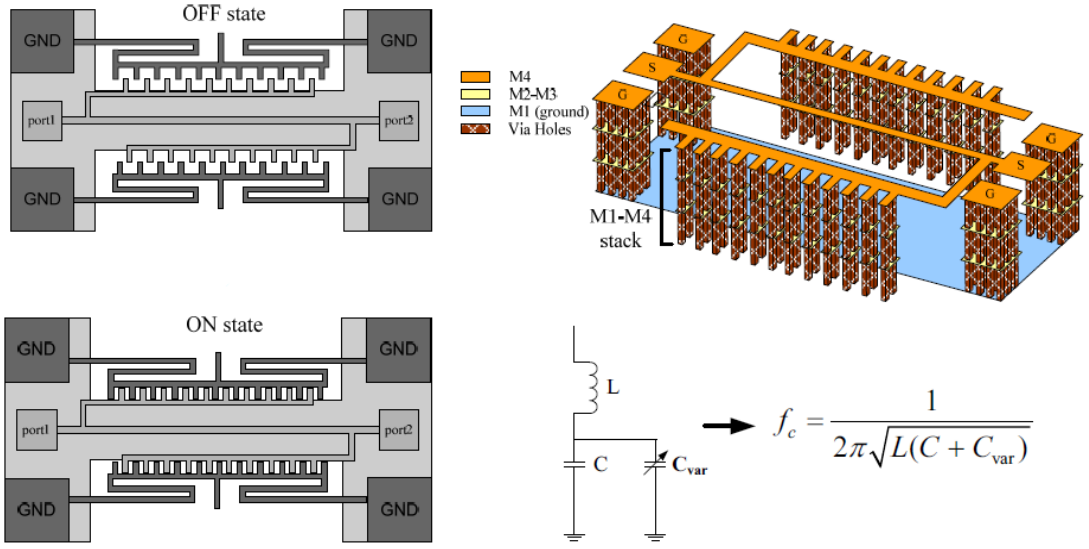


Figure 2-19: Reconfigurable CMOS-MEMS mm-wave band stop filter proposed in [54], using fishbone actuator to adjust open-stub capacitance and thus operation frequency.

Chapter 3

MEMS Fabrication on CMOS 0.35 μm Chips

3.1 Post-processing BEOL layers of CMOS 0.35 μm

Among CMOS-MEMS integration methods introduced in chapter 2, we focus on using the mask-less four-step post-processing technique devised locally by the CIRFE group to release MEMS structures as circuit components from BEOL interconnecting metal layers (see Figure 2.3). Since no extra lithography or deposition step is required, the process is more reliable and consistent in comparison with typical MEMS fabrication methods.

Although the post-processing method can be applied to any commercial CMOS technology with at least four metal layers, we confine ourselves here to TSMC 2P4M 0.35 μm technology. There are four Aluminum layers, denoted as M_1, M_2, M_3 and M_4 (M_1 being the closest to the substrate), and two Polysilicon layers, all surrounded by oxide on top of a Silicon substrate. The topmost metal layer, M_4 , is used as a hard mask to protect structural layers (on M_3, M_2 or M_1) and is eventually removed. The M_2 layer is used as a sacrificial layer. Existing Polysilicon layers are mainly used to create high resistivity bias lines for an electrostatic actuation or for a DC current path when electrothermal actuation is needed. Post-processing includes the following steps:

- Silicon dioxide (as well as passivation Silicon nitride) is anisotropically etched by CHF_3 plasma Reactive Ion Etching (RIE). Each of the metal layers acts as an etch-resistant mask to protect the underlying structures. Oxide from the areas not covered with a metal mask is removed all the way down, so that either the substrate or the sacrificial metal layer is exposed and ready to be etched in the subsequent steps. It is important to remove the post-RIE polymer residue at the end of oxide etching, which can be done by cleaning the chips in the EKC solution.
- A time-controlled RIE of exposed Silicon in SF_6 plasma makes an air trench in the order of $60 - 100\ \mu m$ (depending on the application and design requirements) inside the substrate. This step is important in RF applications to remove the lossy CMOS substrate underneath transmission lines.
- The sacrificial metal layer (M_2), which was the one extending the mask layer (M_4), was exposed following the oxide etch step and is now sacrificed in a (16:1:1) phosphoric–acetic–nitric (PAN)-

based wet etching solution. When M_2 is sacrificed, an air gap is created and structures on M_3 can be released. It is crucial that the top mask layers extend beyond the structural layers by a few microns so that the oxide walls surrounding the structures can protect them from the wet etchant. The mask layer is also removed at this stage. Samples should be immersed in H_2O_2 so that the TiN adhesion layer is etched away. It is possible to add another step to the wet etching and use diluted potassium hydroxide (KOH) solution to get rid of the pile of Silicon remaining in the trench from the dry etch step. To avoid stiction and for better release, this step should be followed by drying the chips in a critical-point dryer (CPD) system.

- The last step is another RIE to remove the top oxide. This is especially important to expose RF or DC pads to make electrical contact possible. The released structures on M_3 are flat prior to this stage. To create an upward deflection in the beams or plates the very top oxide has to be removed.

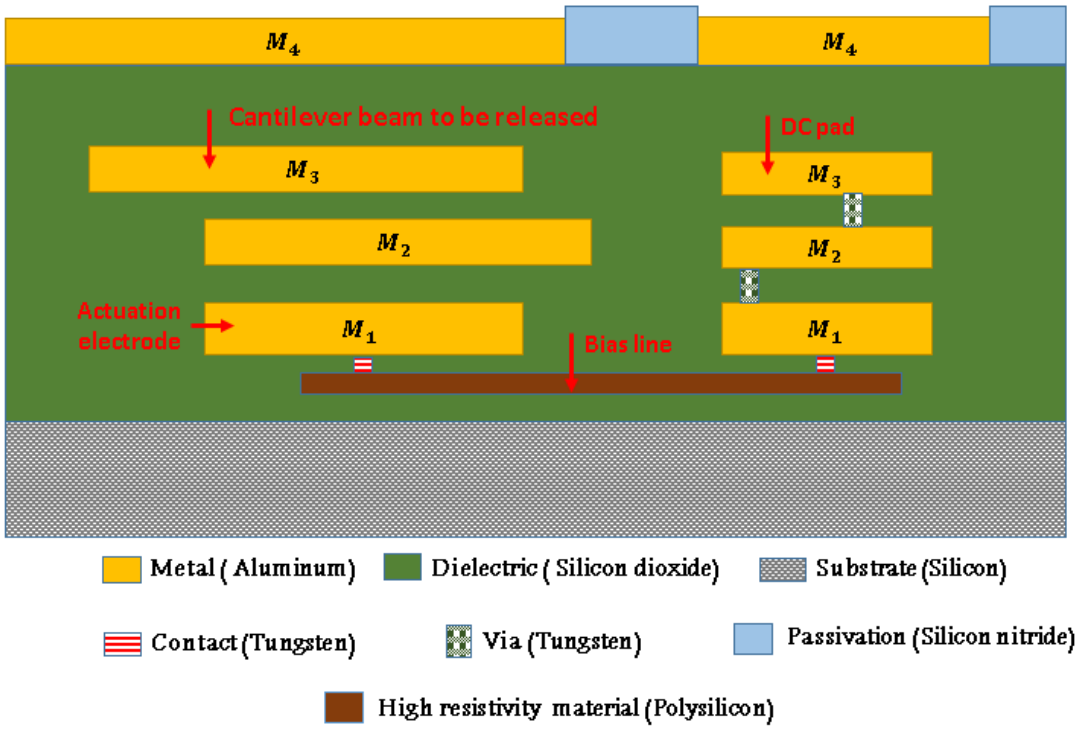


Figure 3-1: Cross section of a chip from which MEMS structures including a cantilever beam, an actuation electrode and a DC pad can be created by post processing.

Figure 3.1 illustrates a simple case where a cantilever beam over an actuation electrode is desired. The beam and the electrode structures need to be fully covered by M_4, while the sacrificial layer in between

should be extended beyond the mask so the beam can be released. A highly resistive Poly line, connected to M_1 by means of Tungsten contacts, creates a path between the electrode and a pad placed on another side of the circuit where the DC probe lands for actuation. Tungsten vias are available to connect metal layers on different levels, if required.

3.2 Mechanical analysis for prediction of post-release deflection

Residual stress and stress gradients inside thin films are inevitable in most deposition processes. Thermal mismatches between metal and dielectric materials in the CMOS process lead to the development of internal residual stress inside layers that can then cause deformation and deflection when structures are released. Due to the difference in the residual stresses of Al and SiO_2 (being tensile and compressive, respectively) from the fabrication process [20], the bi-layer plates or beams typically warp upward after the release step. This warpage can be taken advantage of in many cases. For instance, if plates are to be actuated to work as a switch, the upward curvature would help enhance the capacitance ratio between the OFF/ON stages and improve performance. However the problem is that stress-induced warpage is not precisely predictable and is subject to change across different chips even from the same foundry. Furthermore, post-processing steps affect the final status of the released beams. For instance, it has been reported that the KOH solution used during the wet etching step to help with the air trench inside the substrate slightly attacked exposed oxide as well, such that the thickness of the layer underneath M_3 (denoted as D_3 in this report) decreased from 1 to about 0.65 μm [47] (the thinner the oxide thickness, the higher the warpage). Also, the timing of post-wet etching RIE that is supposed to remove the top oxide directly determines the deflection profile (the warpage increases if the top oxide is fully etched at this step).

A mechanical analysis was previously carried out on released bi-layer metal-dielectric beams [49], where the deflection of the beams at any position from the anchor was predicted by fitting the measured deflection profiles of some test structures with various dimensions to the following curve:

$$d = \theta x + \frac{\kappa}{2} x^2$$

where angular tilt and bending curvature were reported to be $\theta = 0.000406$ and $\kappa = 0.001409$, respectively. Having Young's modulus and Poisson ratios of metal and oxide presumed as $E_{Al} = 70\ GPa$, $\nu_{Al} = 0.3$, $E_{Ox} = 66\ GPa$, $\nu_{Ox} = 0.17$, the averaged stress gradient was found to be $\sigma_{mis} =$

$\sigma_{Al} - \frac{E_{Al}}{E_{Ox}} \times \sigma_{Ox} = 144.74$ MPa. The residual stress vectors for Aluminum and oxide are concluded to be $[100\ MPa, 100\ MPa, 0]$ and $[-42\ MPa, -42MPa, 0]$, respectively.

The mechanical properties above were used to simulate the stress-induced warpage of the bi-layer structures used in RF switches by the MemMech analyzer of CoventorWare software. Figure 3.2 shows CoventorWare model and mechanical simulation results for a bi-layer plate with release holes to be used in normally-ON switches presented in the next section. Figure 3.3 is the warpage curve for the plate according to the angular tilt θ and bending curvature κ reported above. The CoventorWare simulation and the curve both predict the tip deflection to be about 50 μm.

For switch design, to achieve low insertion loss in the ON state and high isolation in the OFF state simultaneously, it is desirable to guarantee a high warpage for the bi-layer beam/plate so that the capacitance ratio between the Down-state (after actuation) and Up-state (before actuation), defined as $C_r = C_{Down}/C_{Up}$, would increase.

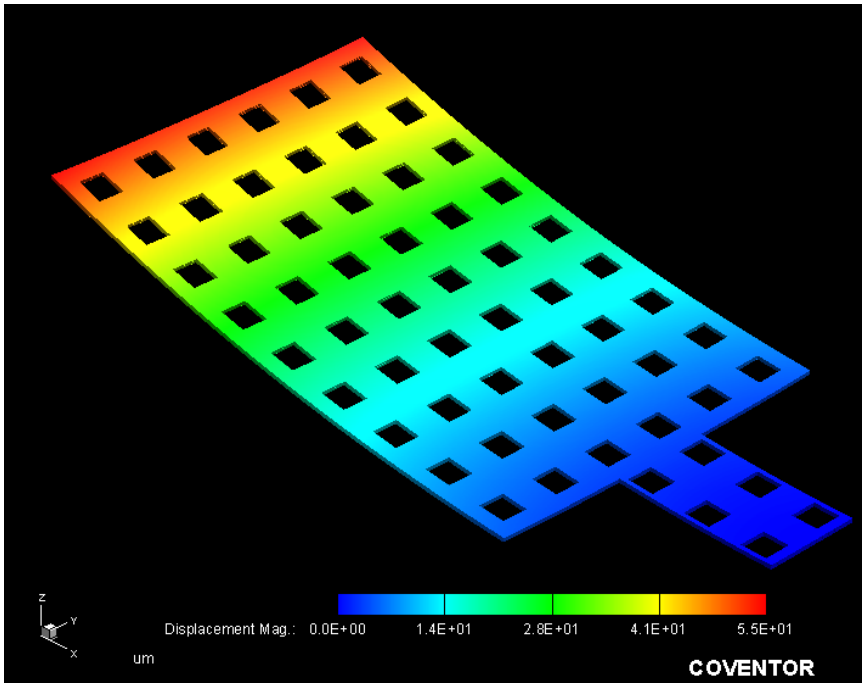


Figure 3-2: Simulated deflection profile after release due to residual stress. The bilayer plate has a dimension of $150 \times 225\ (\mu m)^2$ and is anchored (to CPW line) by a so-called arm $77\ \mu m$ long. Mechanical properties from [49] have been used in CoventorWare analysis.

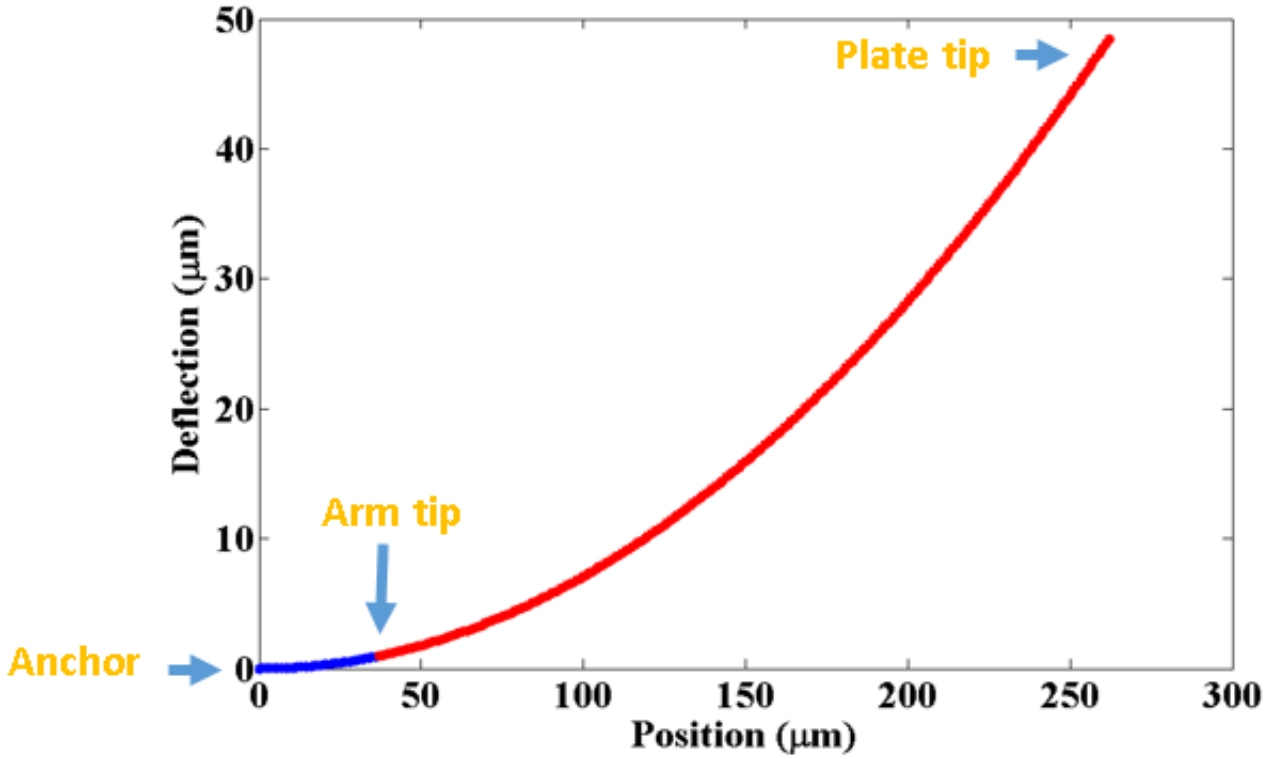


Figure 3-3: Predicted deflection profile for the plate of Figure 3.2 based on curve parameters reported in [49].

Chapter 4

Design and Simulation of MM-Wave MEMS Devices on CMOS 0.35 μm BEOL Layers

4.1 SPST normally-ON shunt capacitive switches

In this section, we report on the design and simulation of electrostatically actuated shunt normally-ON capacitive mm-wave MEMS switches fabricated by standard 0.35 μm CMOS technology. The proposed switch is basically a composite metal-oxide plate composed of M_3 and D_3 anchored to the CPW signal line and suspended on top of the ground plane, forming a shunt capacitor, as shown in Figure 4.1. An electrode under the anchored arm is there to help pull down the structure; applying another DC voltage to the CPW ground plane would bring the plate into capacitive contact and turn the switch to the OFF state.

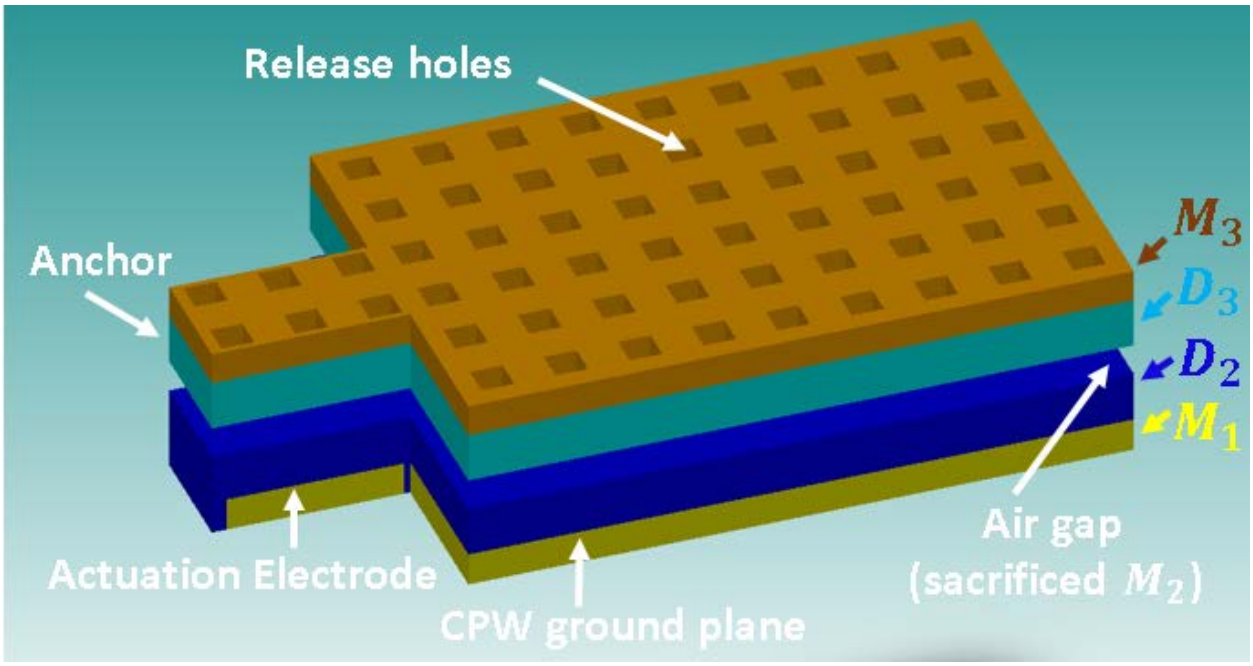


Figure 4-1: Schematic of proposed bi-layer plate of M_3 and D_3 layers anchored to a CPW transmission line and suspended over the ground plane (warpage due to residual stress is not shown here).

The so-called elevated center CPW (EC-CPW) lines are used for all designs by forming a stack of three metal layers (M_1 to M_3 connected by Tungsten vias) as the signal line. EC-CPW has some advantages for this application compared to typical CPW, namely making room to load the line with suspended structures

over the ground planes or MIM (metal-insulator-metal) capacitors and making use of the chip area. The elevated stack line also helps to somewhat reduce conductor losses. The cross-section of any RF current carrying line should be large enough to consider the skin depth of the conductor at the frequency of operation, so that excessive losses are avoided. For 60 GHz and lossy Al of CMOS 0.35 with a conductivity of $\delta = 1.8 \times 10^7\, {}^{S}/_{m}$, the skin depth would be:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = 0.48\ \mu m$$

Therefore, the stack of $M_1/M_2/M_3$, which would be about 4 μm ($\approx 10\delta$), would do the job.

The basic challenge for designing a normally-ON shunt capacitive (SPST) switch would be to have the transmission line loaded with a parallel plate matched to 50 Ω when there is no actuation voltage applied, so that the plates are in the Up position and the switch is said to be ON. A transmission line network with appropriate impedance and length and/or lumped elements should be designed. As will be discussed, there are numerous limitations enforced by either the technology (in terms of cost, material properties, etc.) or the post-processing etch/release stages, which restrict possible options for matching network design.

Matching could be done by several methods, one of which is merely extending transmission line sections from both ends of the plates and adjusting their characteristic impedance and electrical length. Figure 4.2 shows a block diagram of this method. Many sets of solutions might exist for Z_{0_1}, θ_1 , Z_{0_2}, θ_2 to match the switch to $50\ \Omega$. The only concerns would be whether the impedances could be realized in practice and if we can afford the required transmission line lengths for the circuit.

Using the transmission line theory, we find that:

$$Z_{in_1} = Z_{0_1}\frac{Z_{L_1} + j\, Z_{0_1}\tan(\theta_1)}{Z_{0_1} + jZ_{L_1}\tan(\theta_1)} = Z_{0_1}\frac{50 + j\, Z_{0_1}\tan(\theta_1)}{Z_{0_1} + j\ 50\ \tan(\theta_1)}$$

$$Y_{in_1} = \frac{1}{Z_{in_1}} = G_{in_1} + j\, B_{in_1}$$

One approach would be to use a quarter line at one side and then find the characteristic impedance and electrical length of the line on the other side ($Z_{0_1}$and θ_1) in such a way that the effect of the shunt capacitor is cancelled out and the impedance seen by the quarter line is purely resistive:

$$B_{in_1} = -\omega C_{sh_{Up}}$$

$$Z_{L_1} = (Y_{in_1} + Y_{sh_{Up}})^{-1} = (G_{in_1})^{-1}$$

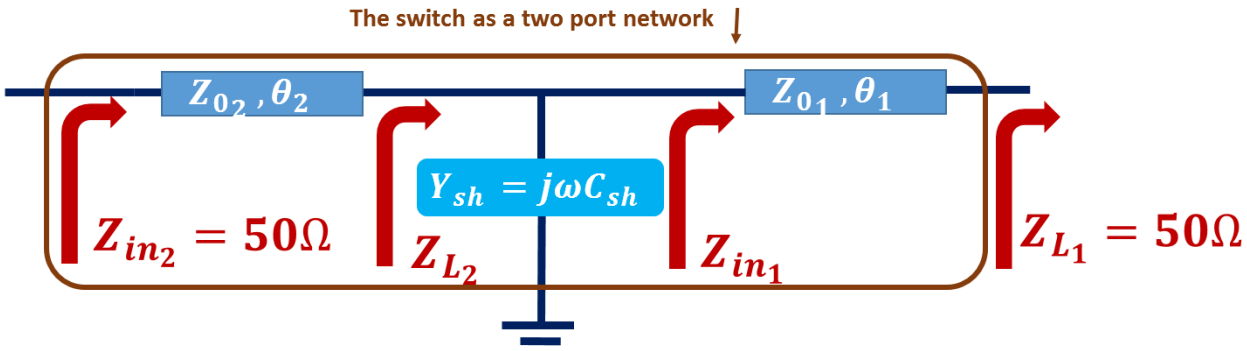


Figure 4-2: Block diagram of one matching method for the normally-ON switch with the shunt capacitor using extended transmission lines.

The quarter line ($\theta_2 = \frac{\pi}{2}$) could transfer the resistive load to a matched one if:

$$Z_{0_2} = \sqrt{Z_{in_2} \times Z_{L_2}} = \sqrt{50(G_{in_1})^{-1}}$$

The circuit OFF-state performance has to be in mind in the meantime. The MEMS plate should have a reasonable size, large enough so the Down-state capacitor to ground would behave as a short circuit at operation frequency ($\omega C_{sh_{Down}} \gg 1$). Since the capacitance ratio between the two states is dictated by the air gap and stress-induced deflection of the plate, there is a limit for the smallest achievable Up-state capacitor value ($C_{sh_{Up}}$).

The above matching method is troublesome for mm wave frequencies where ω and therefore shunt admittance $j\omega C_{sh_{Up}}$ are excessively high. The first transmission line should transform a $50\ \Omega$ load to an admittance for which the imaginary part has a large negative value ($Im\{Y_{in_1}\} = -\omega C_{sh_{Up}}$). As shown in the admittance Smith chart of Figure 4.3, this would be possible only by means of a long ($\theta_1 > \frac{\pi}{2}$) and low impedance ($Z_{0_1} < 50\ \Omega$) line. The impedance/electrical length pairs required to satisfy above condition are compared for 10 GHz and 60 GHz in Figure 4.4. The Up-state shunt capacitor value is assumed to be $50\ fF$ which is in the expected range. For the lower operation frequency, variety of short length high impedance lines can be used, as opposed to the case for 60 GHz.

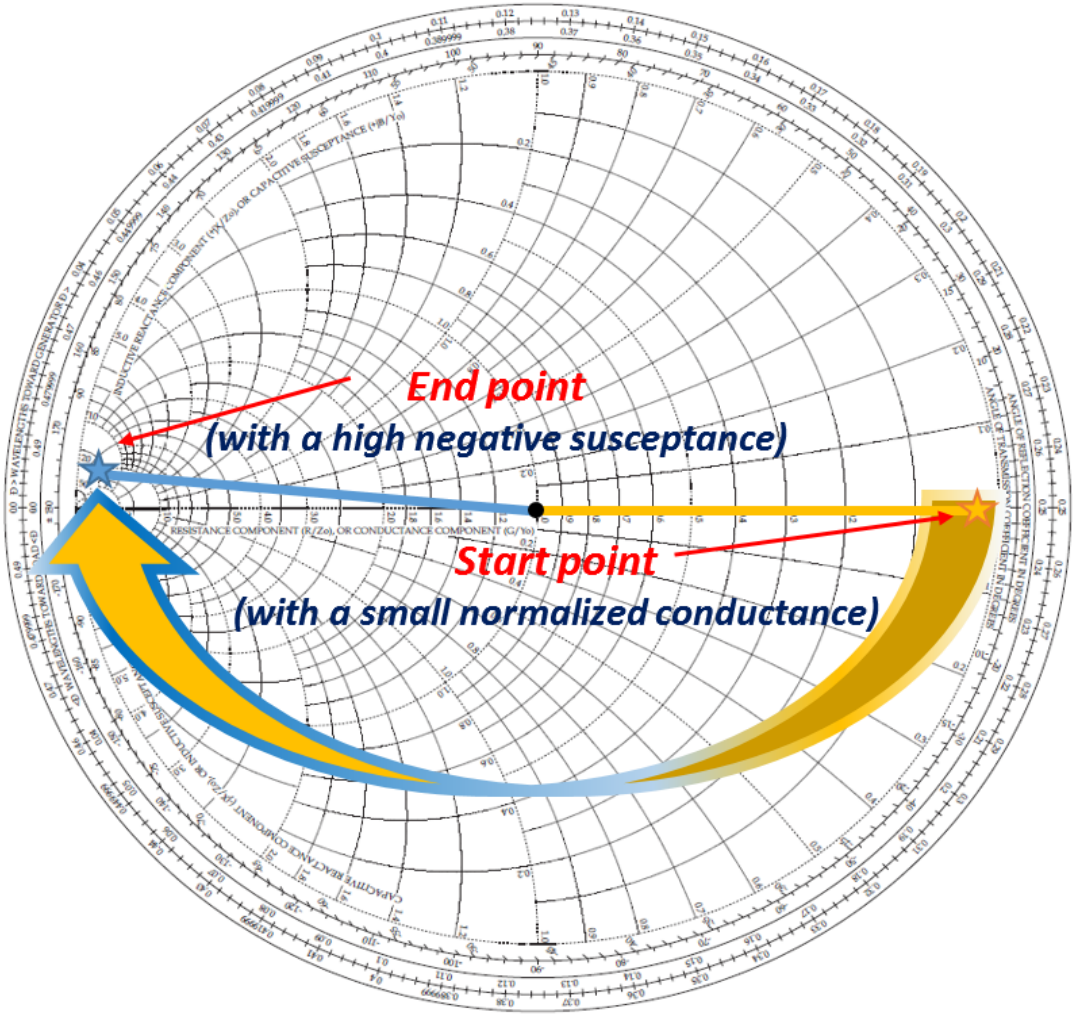


Figure 4-3: Admittance chart used for matching network design. A low impedance, longer than a quarter wavelength transmission line is required to compensate for the effect of a shunt capacitive load in high frequencies.

As mentioned previously, as the losses enforced by low resistivity CMOS Silicon could not be afforded, the substrate under the signal line has to be eliminated. As a result, the effective dielectric constant of the line will be small ($\varepsilon_{eff} \approx \varepsilon_0$), which translates to a high propagation wavelength ($\lambda_g \approx \lambda_0$) and therefore a large circuit size (unless miniaturization or meandering techniques are employed). Moreover, for CPW transmission lines with a low effective dielectric constant, realizing a low impedance requires either an extremely wide line width or a very tiny gap (see Table 4.1), neither of which is feasible to implement. For

instance, if the gap is small, the substrate could not be accessed for post-processing unless some openings are introduced on the signal line to facilitate the etching (but this we would prefer to avoid).

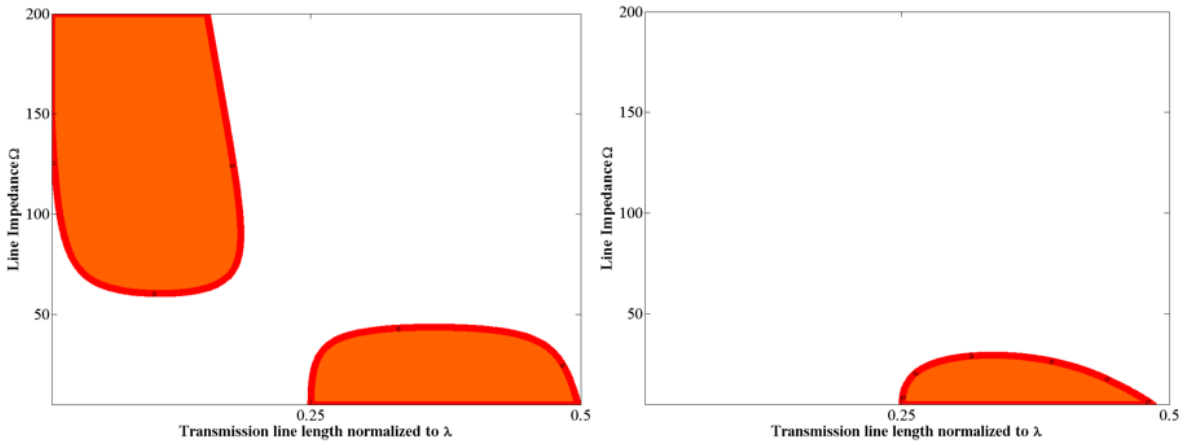


Figure 4-4: Contours for $Im\{Z_{L_2}\}$: red lines track where this value is zero (shunt capacitor is compensated), assuming $C_{sh_{Up}} = 50\ fF$ for (left) 10 GHz and (right) 60GHz.

Table 4-1: Variations of approximate values required for CPW line width (W) and gap size (G) to realize a 50 Ω line in the presence of a deep air trench ($\varepsilon_{eff} \approx \varepsilon_0$).

Z_0 (Ω)	W (μm)	G (μm)
50	60	2.5
	306	6
	980	14

To overcome the issue of matching the parallel plate switch at high frequencies, one alternative method would be to partially compensate the parallel capacitor with a shunt inductor, so that matching with transmission lines of reasonable characteristic impedance and length would be possible. Figure 4.5 shows an equivalent circuit model of the proposed method.

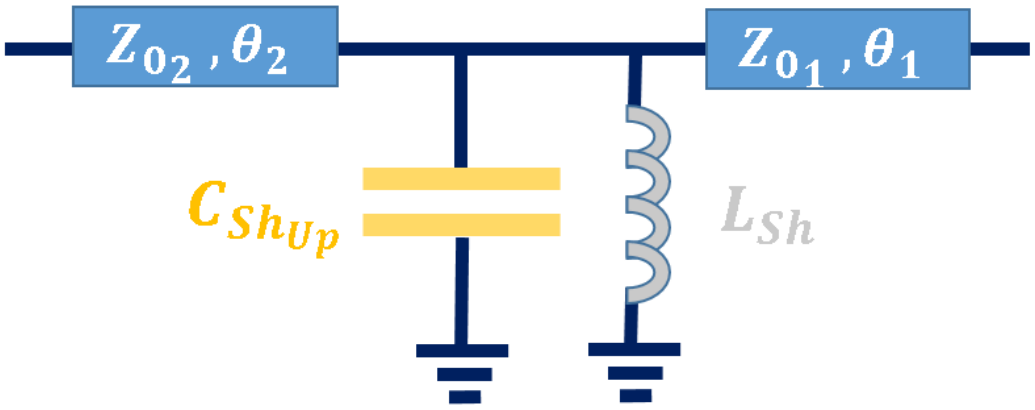


Figure 4-5: Equivalent circuit of matching network for normally-ON switch using transmission lines and lumped parallel inductor.

The first step would be to have a rough estimate of the shunt capacitor to the ground formed by the warped bi-layer plate structure in the Up-state. A numerical method was used to calculate this value from the presumed post-release deflection profile, as follows:

$$C_{Up} = \int dC_{shunt} = \int [\,(dC_{D_2})^{-1} + (dC_{D_3})^{-1} + (dC_{AirGap})^{-1}\,]^{-1}$$
$$= \int [(\frac{dA \times \varepsilon_{oxide}}{T_{D_2}})^{-1} + (\frac{dA \times \varepsilon_{oxide}}{T_{D_3}})^{-1} + (\frac{dA \times \varepsilon_0}{AirGap})^{-1}]^{-1}$$
$$= \int_{X_{Arm}}^{X_{Arm}+X_{Plate}} \frac{\varepsilon_0\, Y_{Plate}}{\frac{T_{D_2}+T_{D_3}}{\varepsilon_{r(oxide)}} + (T_{M_2} + \theta x + \frac{\kappa}{2}\, x^2)}\, dx$$

where $T_{D_2}, T_{D_3}, T_{M_2}$ are the thicknesses of the D_2 and D_3 oxide layers and the M_2 sacrificial metal layer, and $X_{Plate}, Y_{Plate}, X_{Arm}$ denote the dimensions of the plate and the arm holding it over the ground plane. For simplicity, the above formulation does not take into account the release hole openings that would slightly decrease the capacitance value. Using nominal dimensions for the MEMS plate and considering variations for deflection curve parameters (θ and κ), we predict the Up-state capacitor of the plate to be in the range of $15 - 60\ fF$ for the two extreme cases of very high and very low warpage, respectively.

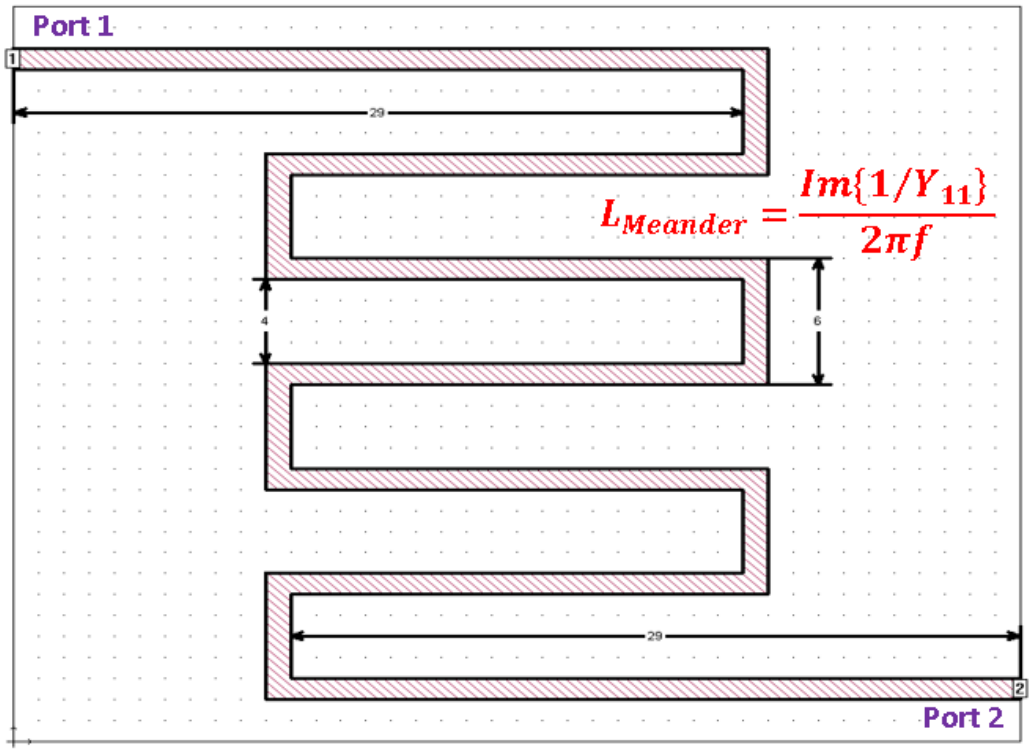
To estimate the order of the required lumped parallel inductor, we go back to the matching problem and put aside the effect of transmission lines at both ends for now. In this case, the circuit is matched if the parallel LC circuit resonates, which occurs at $\omega = \frac{1}{\sqrt{LC}}$. So, for a certain frequency, the smaller the shunt capacitor, the larger the inductor required. Thus, for the frequency and capacitor range that we are dealing

with in this design, the inductor has to be in the order of a few hundred pH, which can be realized by a meandering piece of line connecting CPW to the ground. EM simulation tools (Sonnet and HFSS) were used to adjust dimensions of the meandering line to achieve the desired shunt inductor. Figure 4.6 shows a meandering inductor of about 100 pH; for higher values, the number of legs and/or the spacing should be increased.

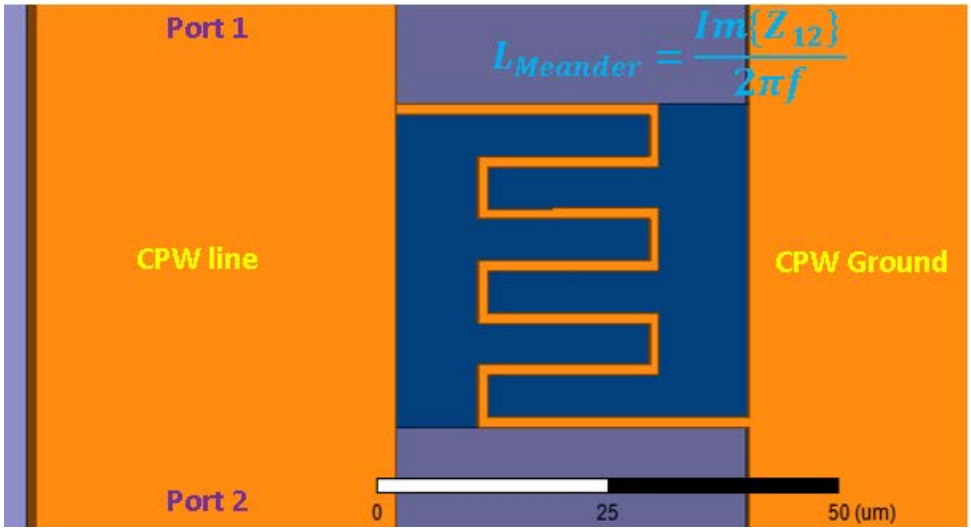
The quality factor of lumped elements is also a concern in RF circuit design. Given that CMOS 0.35 μm BEOL metal layers have low conductivity, using narrow lines could lead to significant losses. In the structure shown in Figure 4.6 (line being 1 μm wide), when metal conductivity and thickness are set to$\sigma = 1.8 \times 10^7\ {}^{S}/_{m}$, and $T_{M_1} = 0.665\ \mu m$, the quality factor defined in Sonnet as $Q = |\frac{Im\{Y_{11}\}}{Re\{Y_{11}\}}|$ would be around 2.7, which is too low.

In considering the equivalent circuit model in Figure 4.5, the length of the transmission lines was set to the minimum possible for economical use of the chip area. Their characteristic impedance depends on the line width and gap size of the CPW line to be fabricated, each having a certain range of practical values for some fabrication considerations (such as avoidance of wide lines or tiny gaps so that substrate etching would be feasible). Considering the above and existence of the air trench, impedances are inevitably high (at least above 100 Ω). So, having an idea about the approximate size and values of different circuit components, we are now ready to build a primary simulation model, the parameters of which can be optimized to satisfy the performance requirements of the switch in both the ON and OFF states.

Figure 4.7 shows the HFSS model used for EM simulation of the EC-CPW line, with a metal stack over an air trench. As described earlier, the Silicon is initially isotropically dry etched around 20-30 μm, after which the wet etching by KOH helps to increase the depth of the air trench to around 60 μm.



(a)



(b)

Figure 4-6: A 7-leg, 1-micron wide meandering line with inductance value of about 100 pH to be used in matching network, designed by (a) Sonnet, and (b) HFSS simulation tools. Dimensions are shown in microns.

The bi-layer warped plate structure of Figure 3.2 previously simulated in CoventorWare, was imported to HFSS as a meshed model for EM analysis. The deflected plate was anchored to a piece of CPW transmission line, and then the simulated S parameters of the 2-port network were used to extract equivalent circuit component values. Neglecting losses, the model is a T-junction consisting of two series inductances (attributed to the transmission line) and a shunt capacitor, a large portion of which is due to the suspended warped plate over the ground plane. Extracted value for the shunt capacitor ($\approx 50\ fF$) was used to replace the imported densely meshed structure with a simple HFSS model of a curved plate to be used in EM simulations. Figure 4.8 illustrates some details.

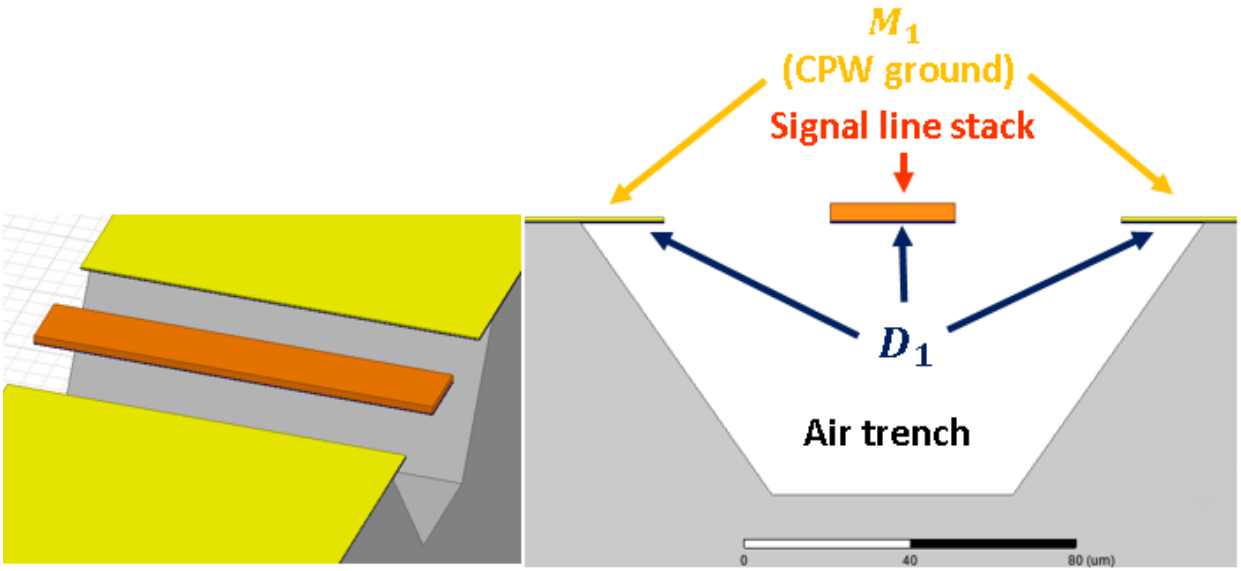


Figure 4-7: HFSS model of the EC-CPW line over the air trench.

The last remaining step for the normally-ON switch design is to run sets of simulations using the simplified model above to optimize transmission line length as well as meandering line dimensions for a reasonably good Up-state matching. Since a DC voltage has to be applied between the CPW line and ground plane for the switch to go to the OFF state, a meandering line should not directly connect the two but a capacitive contact should be used instead. This was realized by terminating the inductor line with a flat piece of metal (on M_2) over the ground acting as a metal-insulator-metal (MIM) capacitor in series (C_s), as shown in Figure 4.9. The equivalent shunt inductor would be decreased unless this plate is sufficiently large to act as an RF short circuit to ground.

Since the deflection profile of the released structure could not be well predicted, the value of $C_{Sh_{up}}$ in the equivalent circuit model of Figure 4.5 is not precisely known. Hence, a variation of matching networks should be tried. This was done by submitting designs with various dimensions for the MIM capacitor.

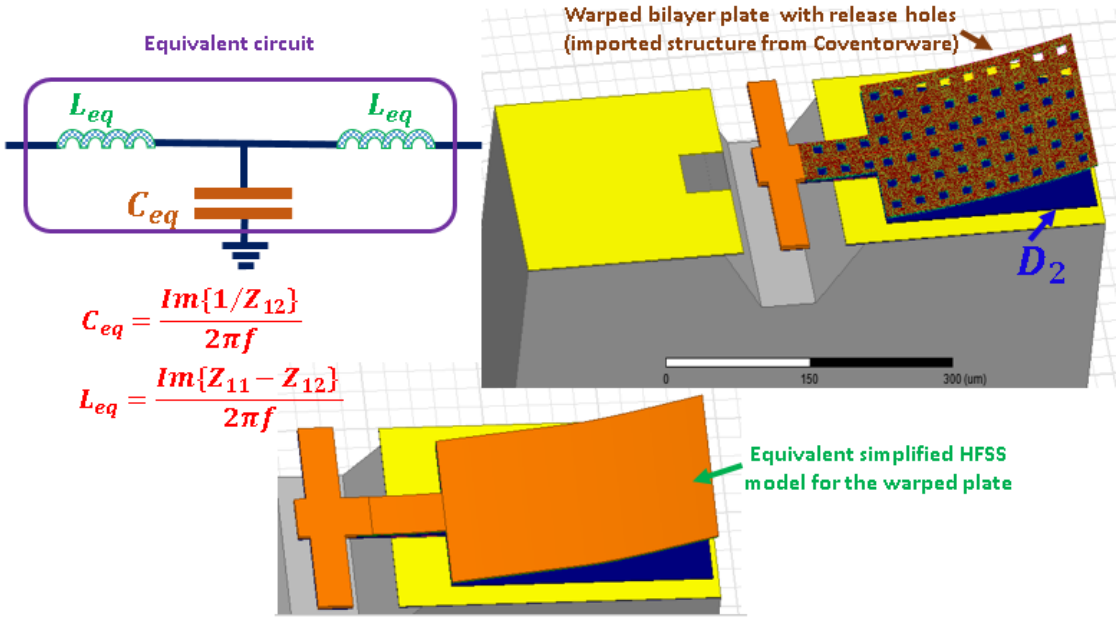


Figure 4-8: A deflected plate model imported from CoventorWare used to extract equivalent circuit values and construct a simplified HFSS model.

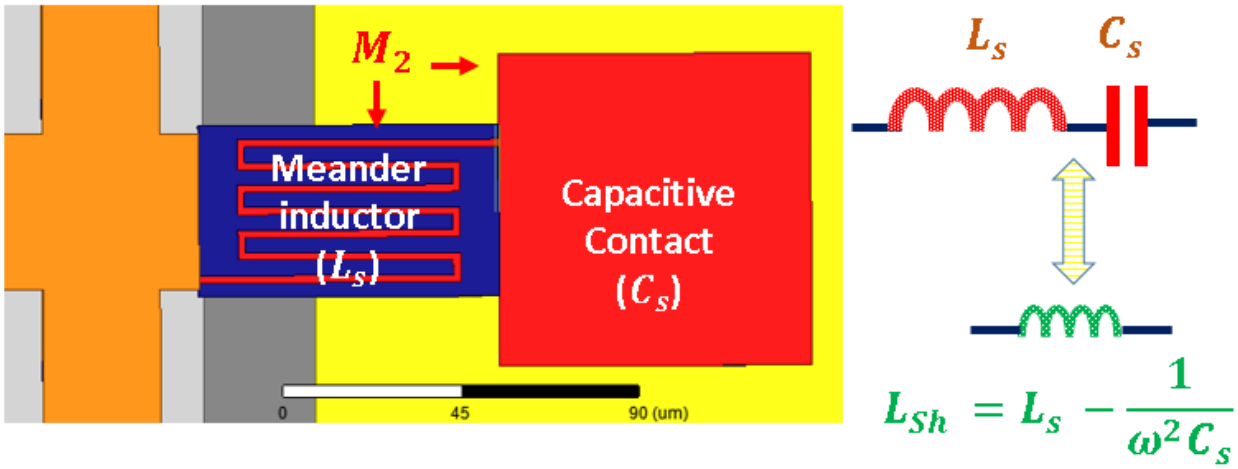


Figure 4-9: Meandering line with capacitive connection to the ground plane to avoid DC short circuit.

Figure 4.10 shows an optimized design model of a normally-ON switch in both states (for the simulation model of the OFF-state in which the beam and the plate are totally pulled down, see Figure 4.11). To be able to eventually test the switch circuits with a PNA network analyzer, there needs to be a pair of 50 Ω RF pads over the substrate on which the G-S-G probes can safely land for RF measurement. We locate the RF pads on M_3 (rather than using the three-layer signal line stack), so distance from the lossy Silicon substrate is maximized. Nevertheless, measured insertion loss of the final switch prototype deteriorates to some extent. There are techniques such as the so-called "Thru-Short-Open" de-embedding method to exclude the effect of lossy pads and obtain S parameters of the DUT by itself (some predesigned dummy patterns on the substrate are tested, then an RF simulation tool like ADS (Advanced Design System) can be used for de-embedding calculations). Figure 4.12 shows EM simulation results (S parameters) of the final normally-ON switch, designed to operate in the 60 GHz frequency band, including the RF pads, and taking into account the effect of non-ideal materials in CMOS 0.35 μm technology (in which electrical conductivity values for Aluminum and Silicon are $\sigma_{Al} = 1.8 \times 10^7\ {}^{S}/_{m}$ and $\sigma_{Si} = 12.5\ {}^{S}/_{m}$, respectively).

A few other variations of this type of switch were submitted for fabrication. For instance, to increase the mechanical stiffness of the beam and prevent breakage during the wet etching step, as observed in some cases, the width of the holding arm was increased (the actuation voltage is expected to increase as a result). As well, we tried increasing the plate size to enhance the capacitance ratio between the two states and improve the OFF-state isolation. In this case, a smaller equivalent shunt inductor would be required for matching, which means a wider meandering line with fewer turning legs should be used. This would decrease conductor losses as well. Figure 4.13 shows the HFSS model and simulation results of this variation.

It is fairly straightforward to adjust the circuit dimensions for the operation at any other mm-wave frequency of interest, such as 77 GHz, for which plate size and shunt inductor values need to be decreased to realize matching in the Up-state. A few additional designs (not shown here) optimized for this higher frequency range are submitted for fabrication.

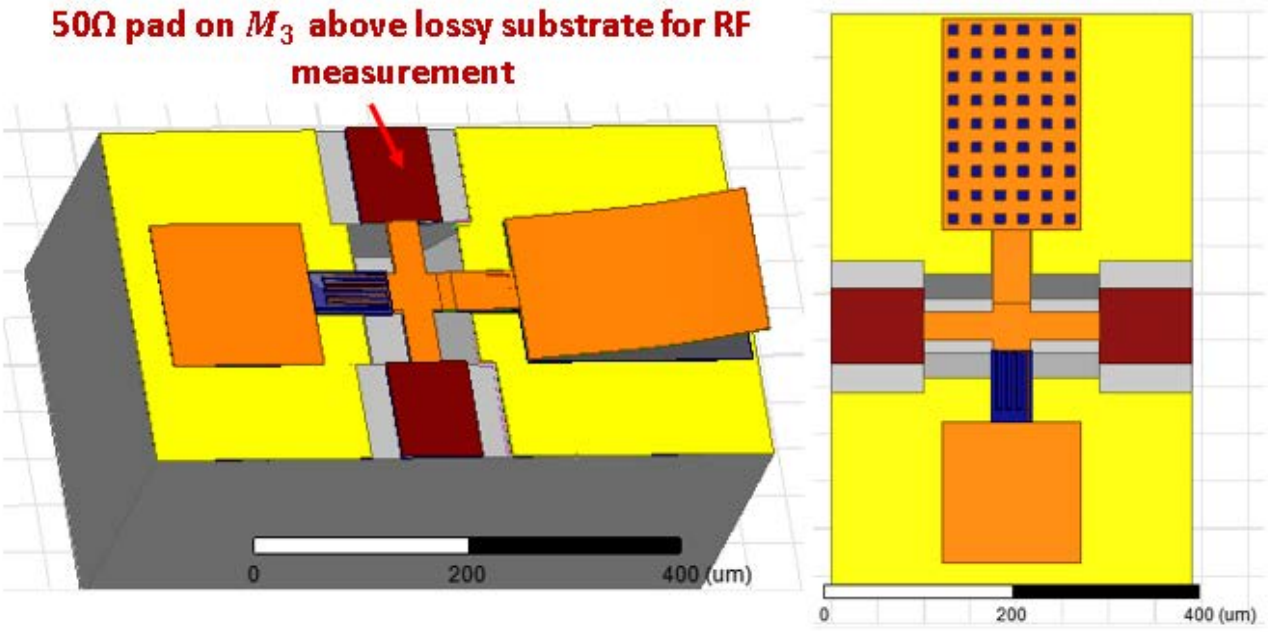


Figure 4-10: Final simulation models for normally-ON switch structure in Up and Down states.

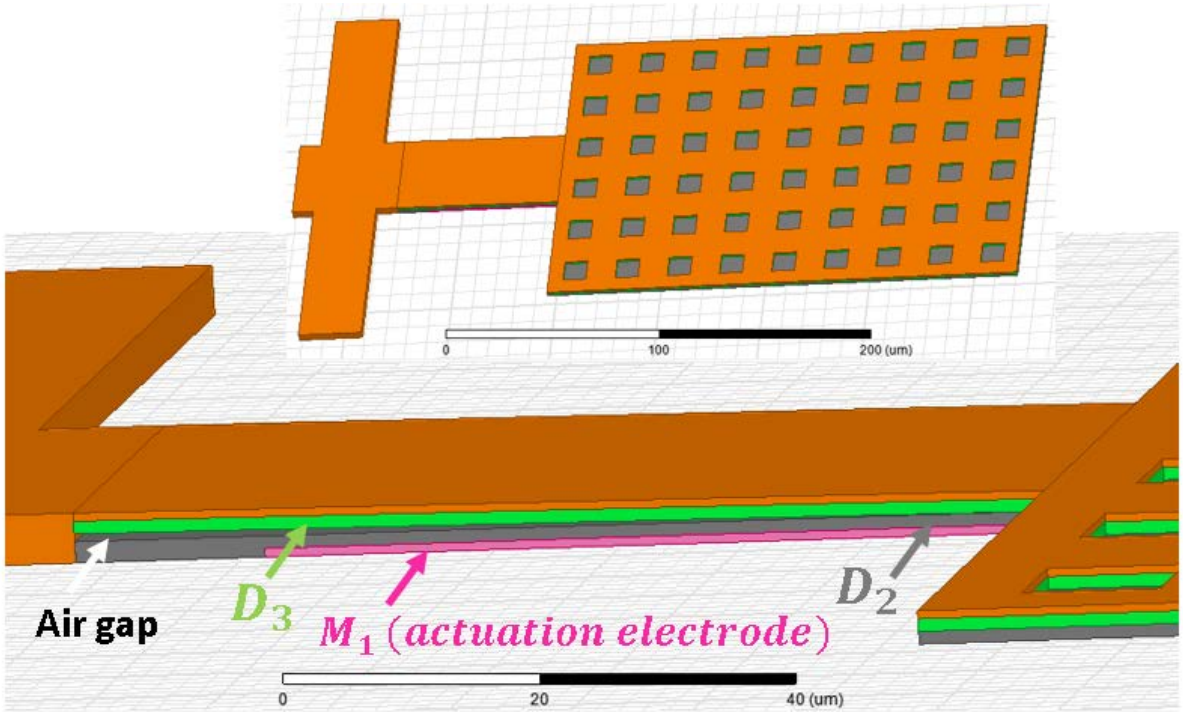


Figure 4-11: HFSS model for the OFF-state.

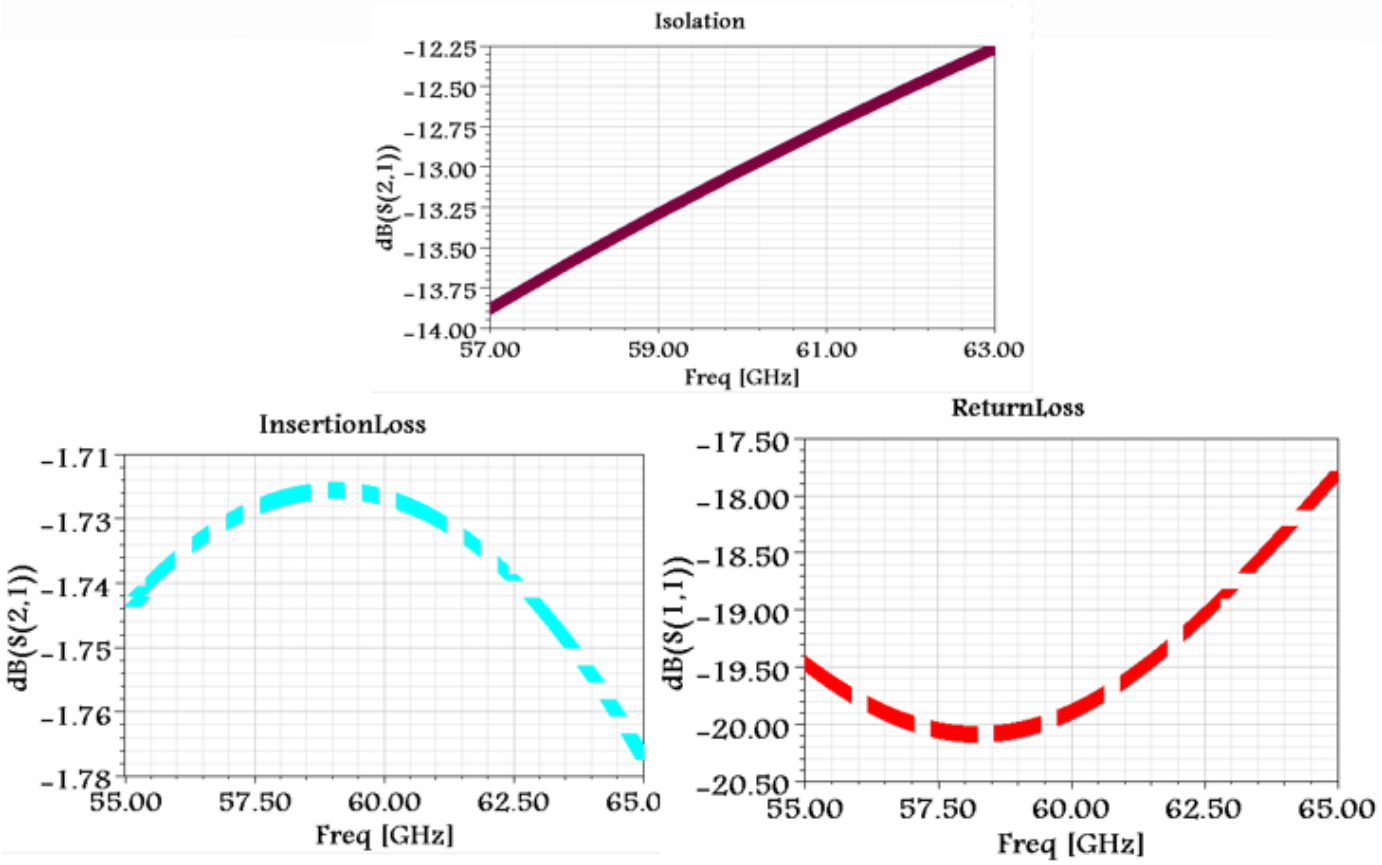


Figure 4-12: Simulated switch performance of the structures shown in Figures 4.10 and 4.11 (material losses are taken into account)

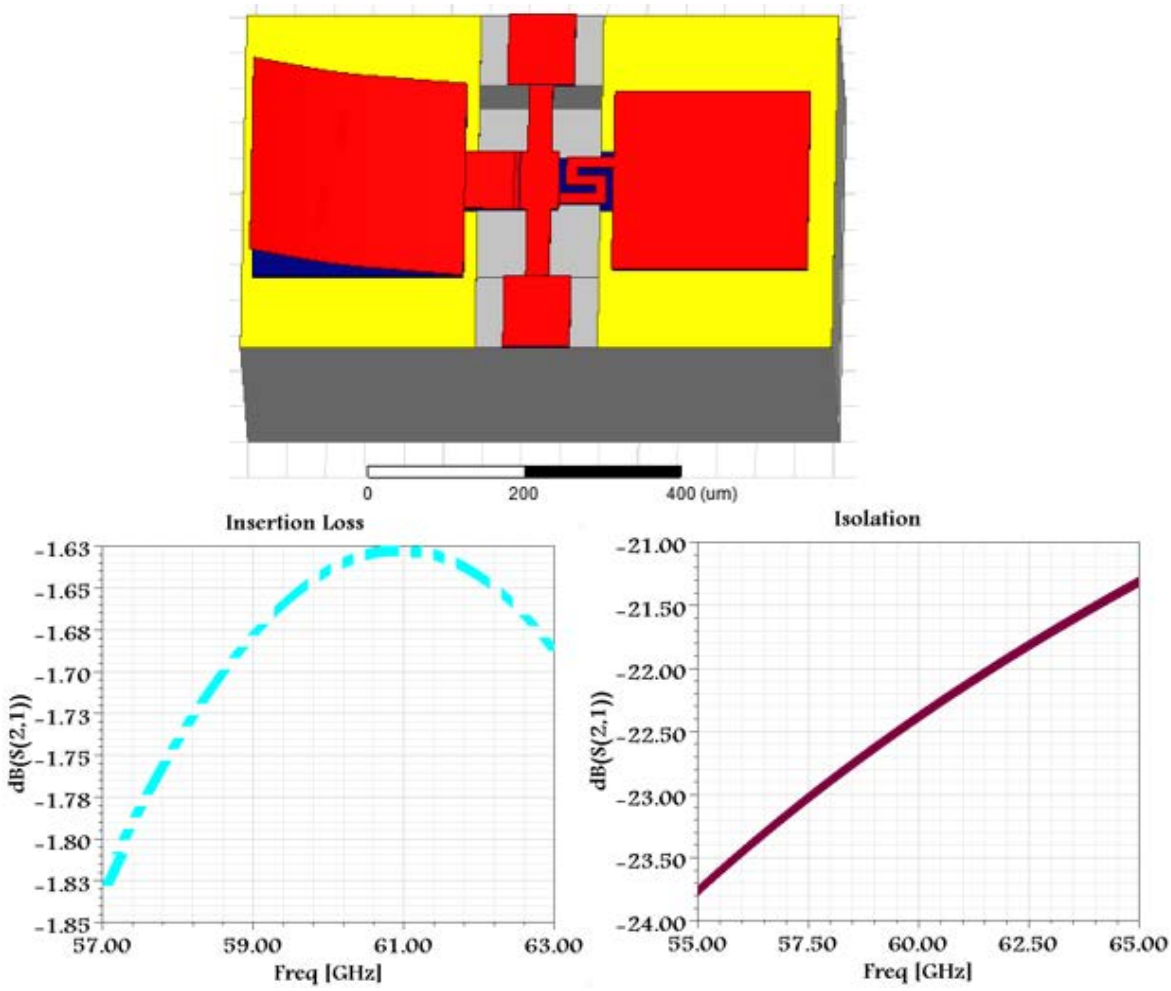


Figure 4-13: A variation of normally-ON switch with a stiffer holding arm and increased plate size ($270 \times 270\ (\mu m)^2$) with improved OFF state isolation.

4.2 SPST normally-OFF series capacitive switches

Normally-OFF series switch designs presented in this section are some improved alternative structures proposed to overcome the following problems experienced with the normally-ON shunt switches:

- The Achilles heel of the normally-ON switch design is that the center frequency of operation would be highly sensitive to mechanical behavior of the bilayer plate. Up-state matching with a lumped inductor element occurs only if the plate deflection profile in the final post-processed structure is precisely as presumed in the simulation (which is very unlikely). If the final warpage

is smaller than what predicted, the shunt capacitor value would be larger and the matching frequency shifts down, and vice-versa.

- The normally-ON designs suffer from conductor losses of the narrow meandering inductor lines. To enhance the switch performance, employing low quality factor lumped elements should be avoided.
- Due to their actuation mechanism, the proposed normally-ON SPST switches could not be easily employed as building elements in compound multiport switch structures. Since all circuit parts share the same ground plane and when DC voltage is applied, all the plates would be actuated simultaneously rather than individually.

In the proposed normally-OFF design, a movable released bi-layer structure is used to switch the circuit ON and OFF. However, it acts as a capacitance in series (rather than parallel), bridging between input and output circuit ports. The operation mechanism is that, for the frequency bandwidth of interest, the input port of the switch should see an RF open circuit when the beam/plate structure is in the Up-state and a matched 50 Ω circuit when the actuation voltage pulls down the structure to the Down-state, respectively. Figure 4.14 shows a very basic structure of the proposed normally-OFF switch in the Up-state and important dimensions which need to be optimized. The circuit has three pieces: the first port feeds the input signal line stack, to which the released bi-layer beam is anchored; the second piece is an actuation electrode under the beam where DC voltage would be applied to pull down the MEMS structure and turn the switch ON; and the third piece is the output signal line stack, which is coupled to the input by the series capacitor and by which a second DC voltage could be applied to help snaping the beam. The equivalent circuit model is shown in Figure 4.15.

Down and up state series capacitor values can be calculated from the following expressions respectively:

$$C_{s_{Down}} = \frac{\varepsilon_0 \varepsilon_r W_b \, (L_b - L_m)}{T_{D_2} + T_{D_3}}$$

$$C_{s_{Up}} = \int_{L_m}^{L_b} \frac{\varepsilon_0 \, W_b}{\frac{T_{D_2} + T_{D_3}}{\varepsilon_r} + (T_{M_2} + \theta x + \frac{\kappa}{2} \, x^2)} \, dx$$

where L_b is the beam length, L_m is the margin between the beam anchor and second transmission line section on M_1 (which is a few microns larger than the electrode length L_e), W_b is the width of the beam, and θ and κ are parameters of the quadratic curve used to model the post-release deflection profile of the

beam. As an example, for $L_b = 250\ \mu m$, $L_m = 200\ \mu m$ and $W_b = 30\mu m$, the Down-state capacitance would be around $0.02\ pF$ and the Up-state capacitance (which vary depending on the deflection profile of the beam) is predicted to be smaller than about $1.3fF$. These estimated values were used to analyze the equivalent circuit model of Figure 4.15 by ADS simulation tool. A set of transmission line lengths and impedances could be found to match the circuit in the Down-state.

When the Up-state capacitor is small enough the switch behaves like an open circuit ($S_{11} \approx 1e^{j0}$), provided that the length of the first signal line (L_i), is small as well. There is a trade-off between switch performances in the two states, as for most design parameters (circuit dimensions shown in Figure 4.16) if adjusted in favor of any of the two states the functionality of the other would be deteriorated. Switch performance is highly frequency-dependent. For lower frequencies, it is more important to adjust the model in favor of the Down-state, since the series admittance in the Up-state ($Y_{s_{Up}} = j\omega C_{s_{Up}}$) is already small enough.

A modified structure is proposed to address the tradeoff problem. Terminating the beam with a wider piece of plate helps to increase the Down-state capacitance. However, if the beam is long enough, the displacement of the released structure at the tip would create a large air gap, such that the increase in the Up-state capacitance would be negligible. Another approach is to add a narrow piece of line following the capacitive junction, which does not affect the OFF-state performance but acts as a small inductor in series (L_s) and increases the equivalent Down-state admittance:

$$Y_{eq} = \frac{1}{j\omega L_s + \frac{1}{j\omega C_s}} = \frac{j\omega C_s}{1-\omega^2 L_s C_s} > j\omega C_s \quad (L_s < \frac{1}{\omega^2 C_s})$$

Figure 4.17 shows the final model of a normally-OFF switch (designed to operate at 60 GHz), in its Down-state with 50 Ω RF pads on Silicon, tapered to connect to the narrower lines on both ends. HFSS simulation results, including all sources of loss are presented.

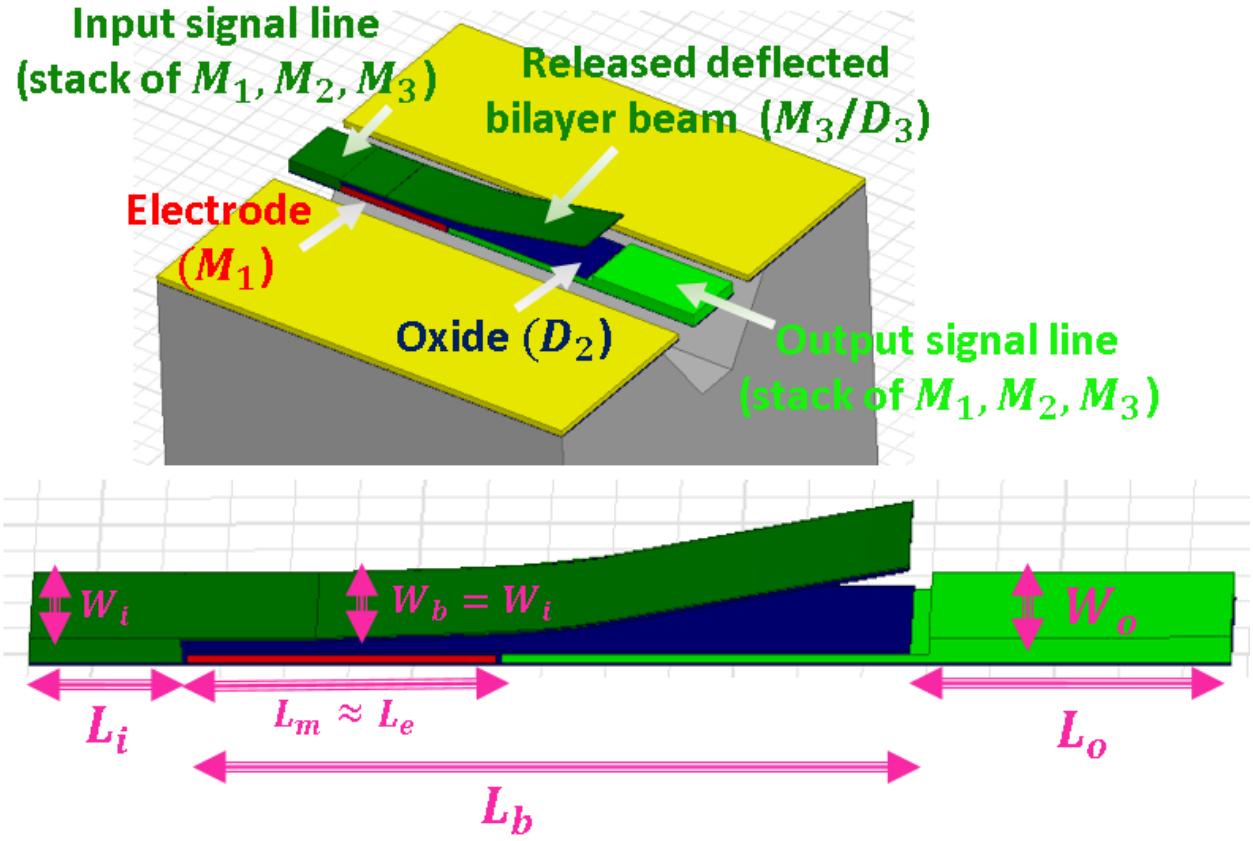


Figure 4-14: Simple version of proposed normally-OFF switch in the Up-state and its important design dimensions.

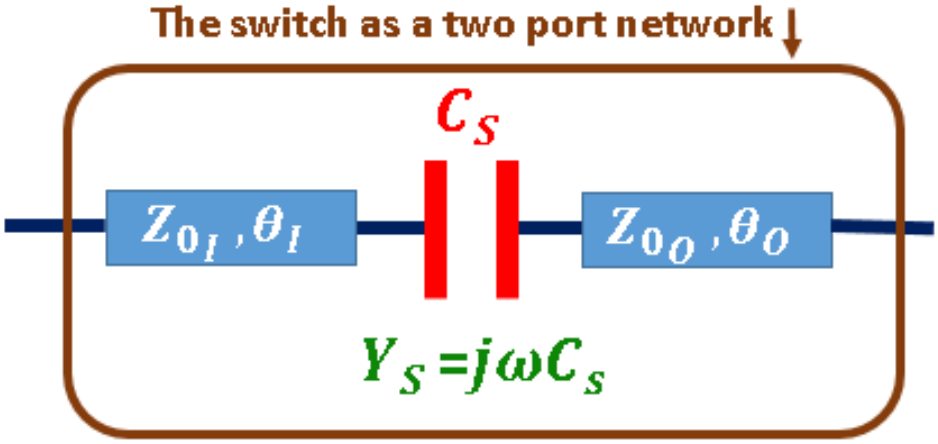


Figure 4-15: Equivalent circuit model of normally-OFF switch with actuating beam/plate as series capacitance between input and output circuit components acting as transmission lines.

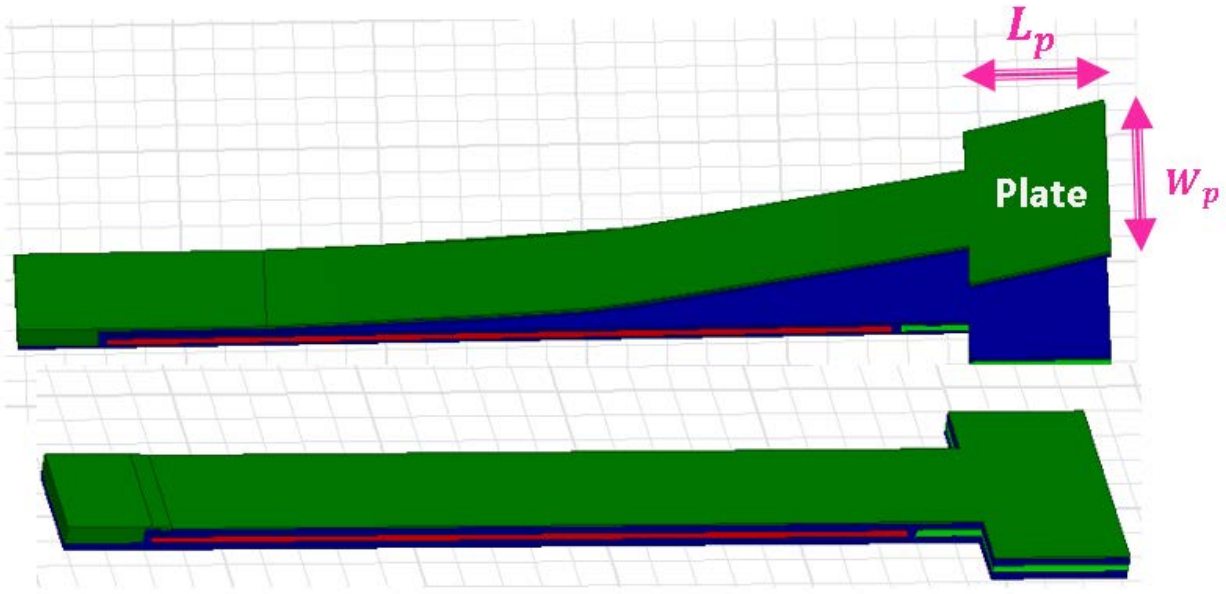
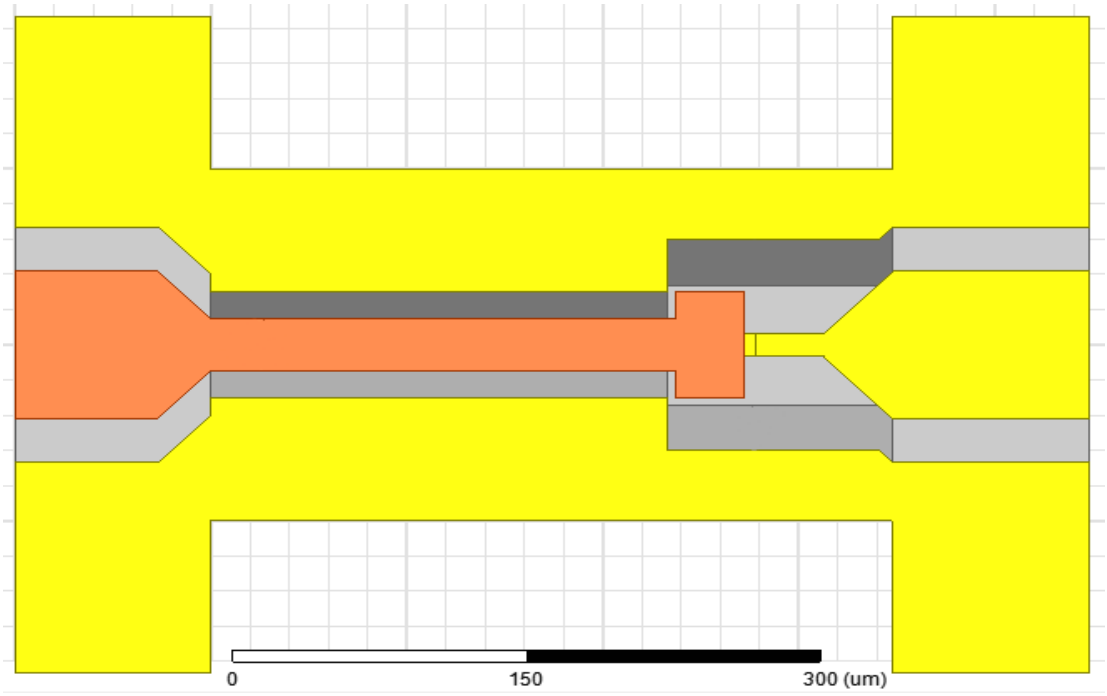


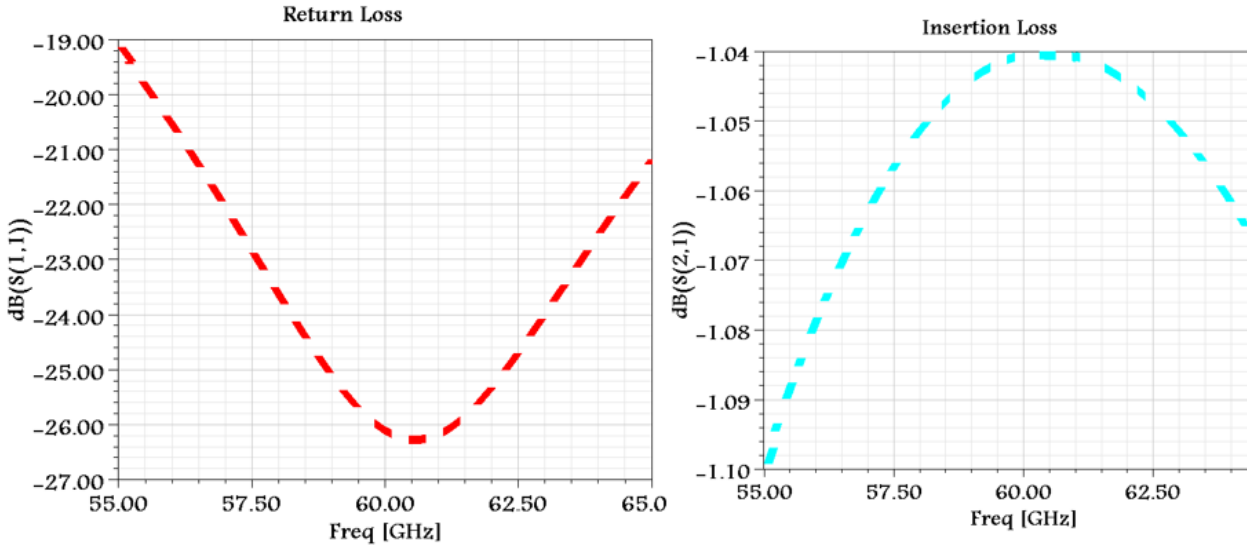
Figure 4-16: Modified beam structure with plate at the end to enhance Down-state series capacitance.

OFF-state performance depends on the post-release deflection of the beam/plate structure. A model has been simulated using an Up-state beam with several different deflection profiles. OFF-state isolation is at least 20 dB for the typical predicted profile (angular tilt θ and bending curvature κ of the deflection curve as reported in [49]), while in the unlikely case of a very low deflection, isolation is still better than 13 dB. It can be concluded that contrary to what we had for the normally-ON switches, the OFF-state performance in the current design is not extremely sensitive to the stress-induced mechanical behavior of the structures, with the ON-state insertion loss being totally independent of that.

Knowing basic principles of switch operation, it is easy to re-design the model to function at any other mm-wave frequency. Let us consider 77 GHz rather than60 GHz. The transmission lines in Figure 4.15 required for the matching network would be favorably shorter for higher frequencies. Although the beam length would not shrink as much since it has to be long enough for a reasonably high tip deflection, there would be no need to exploit a wide plate at the end to enhance Down-state capacitance anymore. As discussed earlier, the higher the frequency, the circuit parameters can be altered in favor of the OFF-state isolation. Figure 4.19 shows a variation of the switch which is simpler and more compact, operating at a higher frequency range.



(a)



(b)

Figure 4-17: HFSS model of final normally-OFF capacitive switch in Down/ON state and its simulated S parameters.

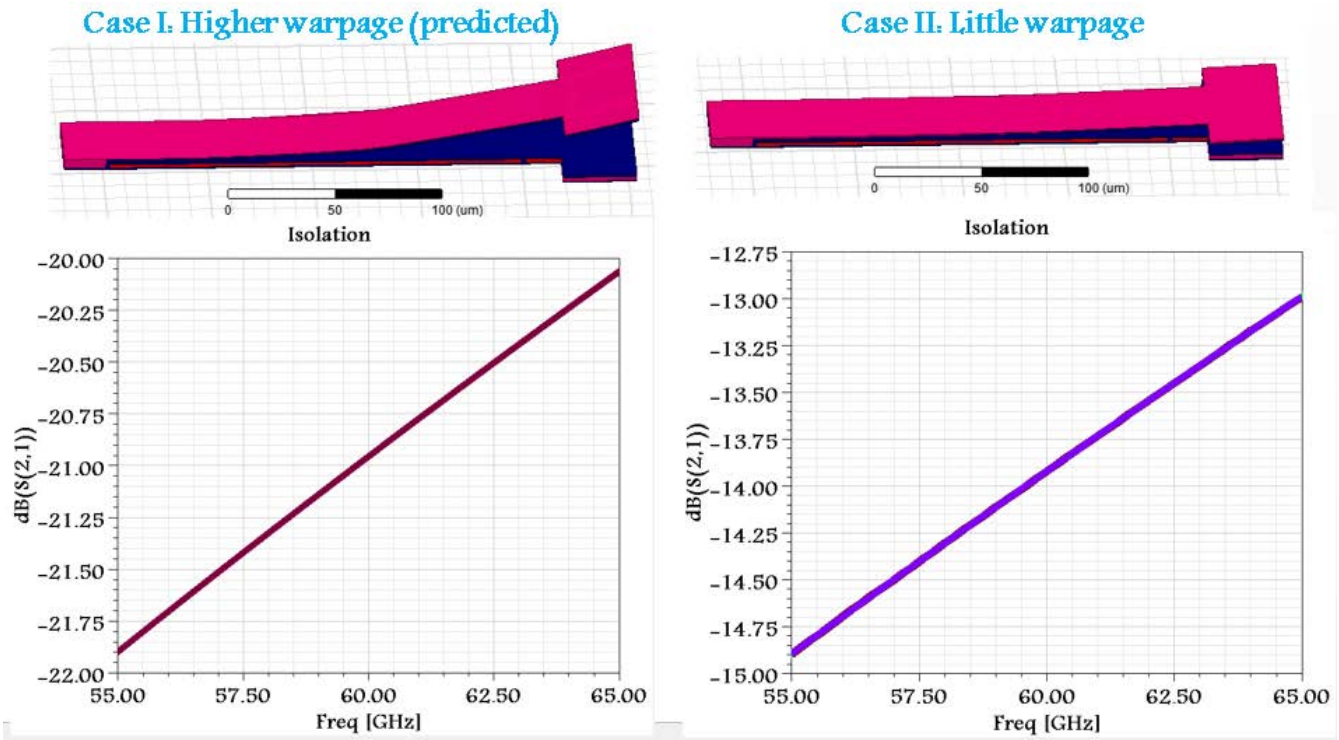


Figure 4-18: Simulated OFF-state isolation of the designed switch in two cases, when upward warpage is as predicted (left) and when it is extremely low (right).

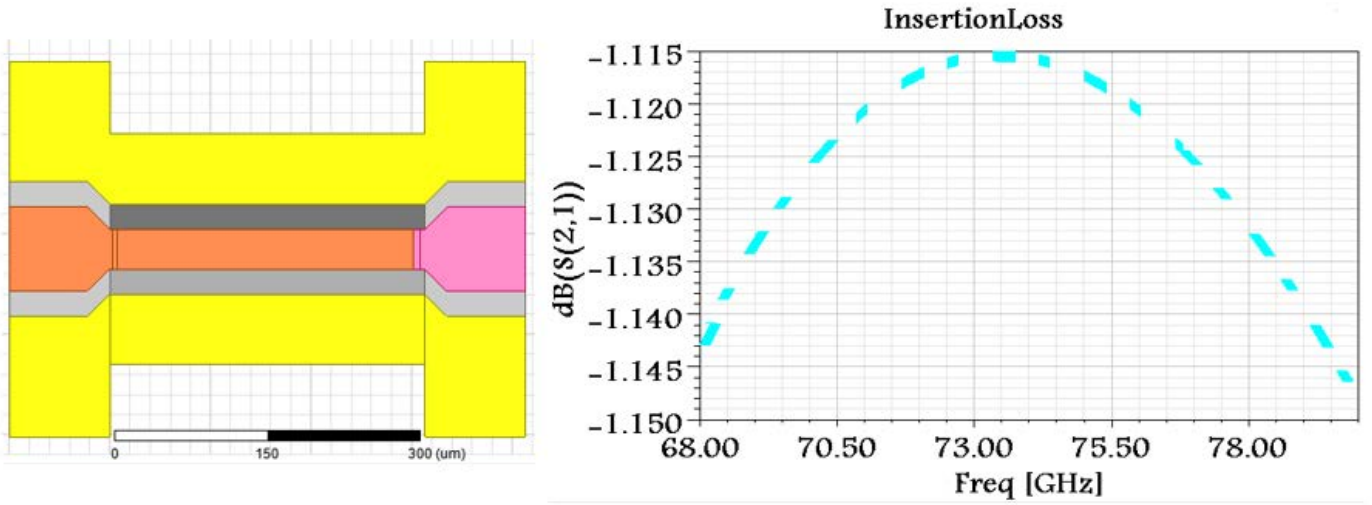


Figure 4-19: A simpler and smaller variation of the RF switch designed for a higher mm wave band.

4.3 SP3T normally-OFF switches

So far, we have focused on single-pole single-throw (SPST) MEMS switches. Now we can move on to the next level. It would be possible to use already-designed structures in a certain configuration to implement a single-pole multiple-throw switch.

The simulated models in Figure 4.21 provide some proof of the concept as well as a starting point to design SP3T switches on a CPW line circuit with a cross junction. The lines are 50 Ω, and the aim is to transmit an RF signal from the input port to the output with minimum insertion loss. This occurs if the input impedance of both branches is infinity. In one scenario branches are half a wavelength each (at the center frequency) and terminated at an open circuit, in the other they are quarter lines connected to the CPW ground. Both models were simulated at 60 GHz.

As an idea of how to realize a SP3T, assuming an ideal case of having SPST switches with perfect performance in both states (acting as short circuit when ON and as open circuit when OFF), one could feed a CPW cross junction similar to what was used in the above models and simply replace branches with switches at the OFF-state and the main line with a switch at the ON-state. However, considering that switches are not ideal and that a 50 Ω line could not be easily realized using our CMOS-MEMS process, some adjustments and parameter optimization would be needed to come up with an acceptable performance. Some radiation loss corresponding to the signal disturbance caused by the circuit discontinuity at the cross junction is inevitable. Use of air bridges of appropriate size to connect the ground planes is recommended or the CPW propagation mode would be lost at the cross junction.

Figure 4.22 shows the top view of a designed SP3T switch model operating around 60 GHz. Any of the three released beams could be electrostatically actuated to transmit an RF signal. Figure 4.23 shows the simulated return loss, insertion loss and isolation of the structure for a case where the middle switch is actuated. The performance of the other scenario, in which a beam at one side is pulled down, is almost similar but slightly deteriorated. A simpler design was optimized to function around 77 GHz, as shown in Figure 4.24.

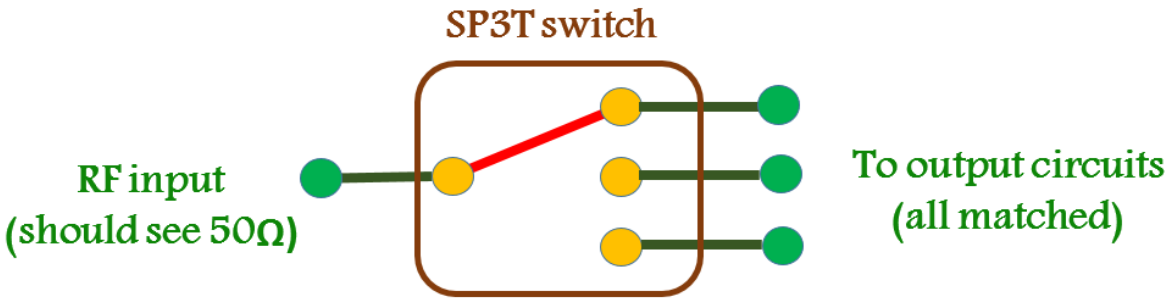


Figure 4-20: Schematic of SP3T switch.

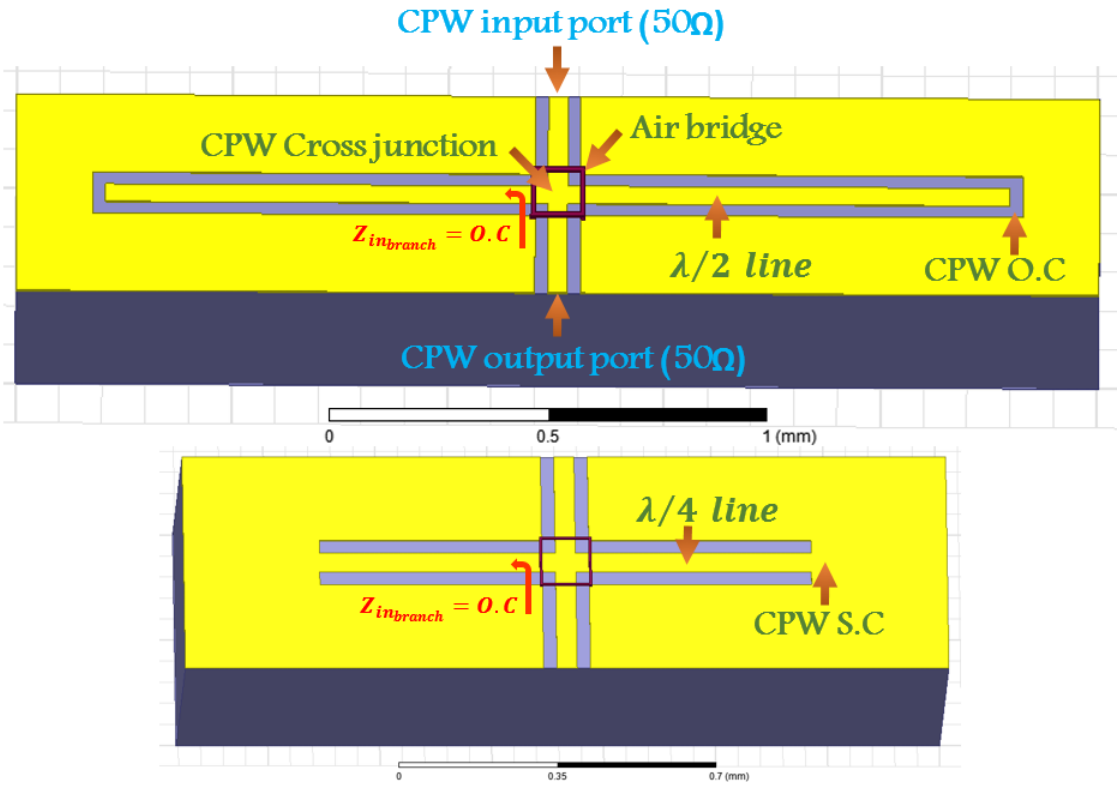


Figure 4-21: Simulated HFSS models used as proof of concept for designing SP3T switch on a CPW line.

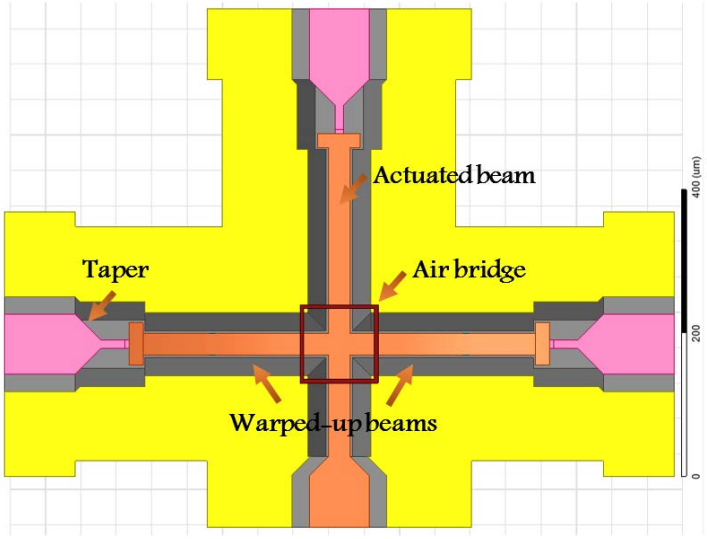


Figure 4-22: HFSS model of SP3T switch for 60GHz band.

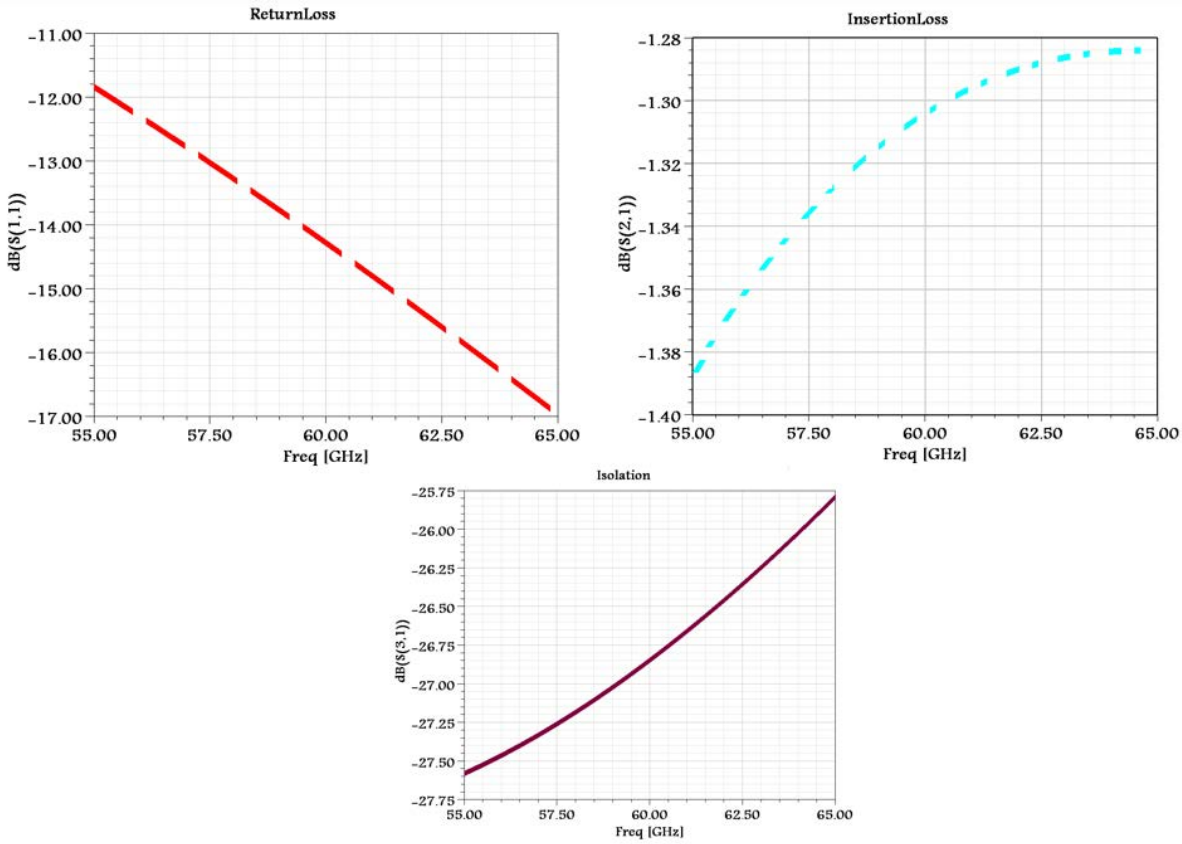


Figure 4-23: Simulated S parameters of the 60GHz SP3T switch.

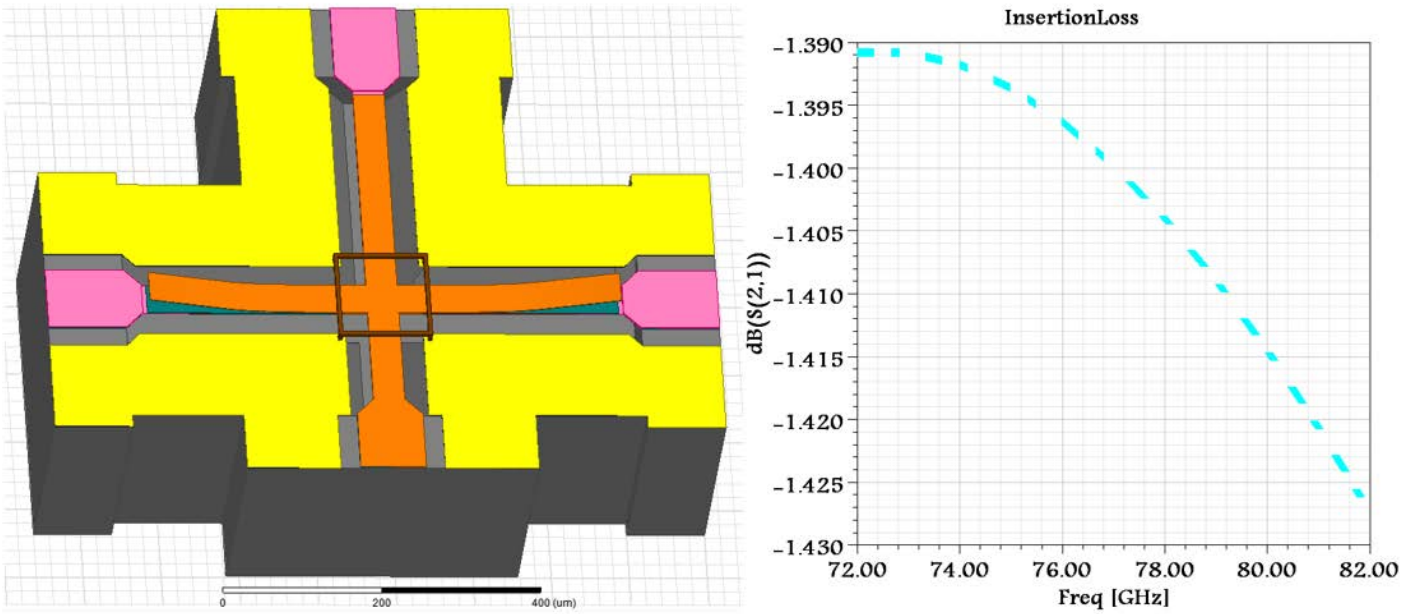


Figure 4-24: HFSS model and insertion loss plot of the 77 GHz SP3T switch.

4.4 Distributed MEMS Transmission Line (DMTL) phase shifter

The idea behind a DMTL phase-shifter is to load a high impedance transmission line with variable/switchable capacitors and make a slow-wave structure. Tuning the line impedance and phase velocity of the travelling wave (so electrical length of the line) is possible by adjusting the loading capacitances. A schematic of the circuit is shown in Figure 4.25, where Z_0 , S and C_{sh} are characteristic impedances of the unloaded line, periodic spacing between the loads, and variable shunt capacitors, respectively.

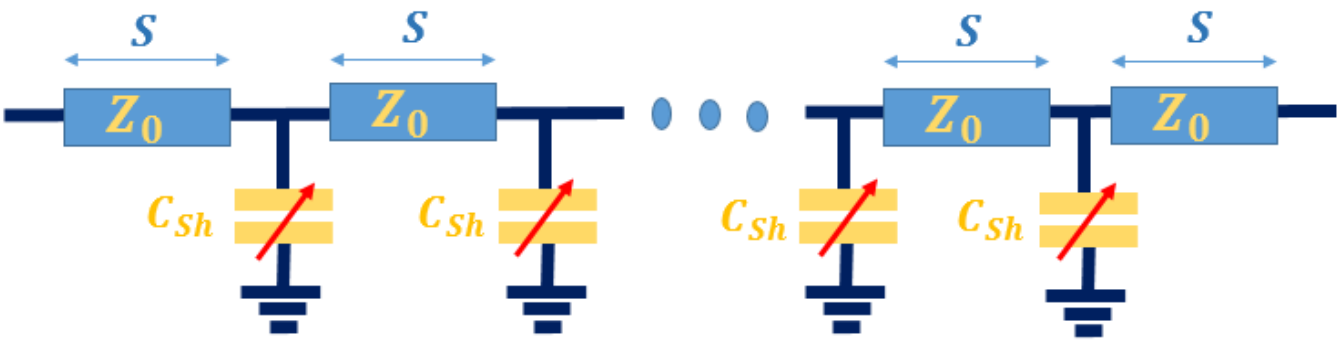


Figure 4-25: Schematic of periodically loaded transmission line with variable capacitors.

Suspended MEMS plates over a CPW ground plane can be used as switchable loading capacitors. Here are some important challenges and trade-offs for DMTL phase-shifter design:

- It is not possible in practice to tune the capacitors continuously by a DC voltage since pull-in occurs at a certain point (plus, the pull-in voltage might not be even consistent due to dielectric charging effects). Thus, only two discrete capacitor values are achievable corresponding to before and after actuation.
- We must have good knowledge of the exact loading effect of the MEMS plates which depends on their post-release deflection profile.
- The characteristic impedance of the unloaded line, spacing between the loads and the suspended plate dimensions should be designed such that the circuit is almost matched to 50 Ω.
- It is important to maintain almost consistent insertion loss in the tuning range of any phase shifter to avoid amplitude distortion. This is hard to achieve for this design, since the loaded transmission line segment cannot be perfectly matched to 50 Ω in both states. The characteristic impedance of the loaded line (so the return loss) varies when capacitors are switched.
- The amount of phase shift each segment of the loaded transmission line offers depends on the capacitance ratio between the states: the higher the ratio, the greater the shift in phase. However maintaining a good matching at both states would be more difficult.
- DMTL is a periodic structure and there is an upper limit for the frequency of operation due to Bragg reflection [72]: $f_{Bragg} = \frac{1}{\pi S\sqrt{L_t(C_t+C_{Sh}/S)}}$, where C_t and L_t are per unit length capacitance and inductance of the unloaded transmission line. The characteristic impedance of the loaded

line would drop close to Bragg frequency [73]: $Z_{0L} = \sqrt{\frac{L_t}{C_t + C_{Sh}/S}} \times \sqrt{1 - (\frac{f}{f_{Bragg}})^2}$. One requirement would be to push the Bragg frequency way beyond the frequency of operation, otherwise the system would become nonlinear across the frequency band.

- The chip area is another concern. Each DC pad, which needs to be at least $100 \times 100\ (\mu m)^2$, can control several cascaded segments corresponding to a single bit of the phase shifter. For instance, to realize a 4-bit 90° phase shifter, four DC pads are required and the number of segments controlled by each should be large enough to provide $\Delta\Phi_{Bit}$ =90° of phase shift.

Figure 4.26 shows an equivalent per unit length lumped element model of loaded versus unloaded transmission lines and the relationship between per unit length intrinsic inductance and capacitance values (L_t , C_t), per unit length extra loaded capacitance ($C_t{}^+$), characteristic impedance values for both cases (Z_0, Z_{0L}), and the phase velocity of the loaded line (u_{pL}).

Figure 4.27 shows HFSS model of a CMOS-MEMS high impedance CPW transmission line segment over an air trench and loaded with capacitive plates. The primary design concern is to match each individual section by optimizing appropriate values for the unloaded line impedance Z_0, shunt capacitor values imposed by suspended plates $C_{sh} = 2C_{Plate}$, and the spacing between adjacent loads S. In the equivalent circuit model of Figure 4.26, the extra loaded capacitance value can be considered as $C_t^+ = \frac{C_{Sh}}{S} = \frac{2C_{Plate}}{S}$. Following the equations, theoretical values for S and Z_0 are found for a perfect matching ($Z_{0L} = 50\ \Omega$) as presented in Figure 4.28. Also, considering the predicted deflection profile of the bi-layer released plates, an approximate value for the shunt capacitor is found for any dimensions, as seen in Figure 4.29. The above calculations were performed to achieve some primary values to design a DMTL circuit.

The design is rather challenging, since we would require a good matching condition for both states for when the plates are Up and also when they are actuated. On the one hand, the higher the ratio between capacitor values, the more phase shift can be obtained between the states, while on the other hand, a drastic change in loading capacitor deviates equivalent characteristic impedance of the line from 50 Ω and imposes a high insertion loss.

Figure 4.30 shows HFSS model for the final DMTL design with 10 cascaded segments acting as a single bit phase shifter. DC voltage should be applied between the main line and the ground plane to actuate the plates. Simulation results (with all lossy materials taken into account) are shown in Figure 4.31.

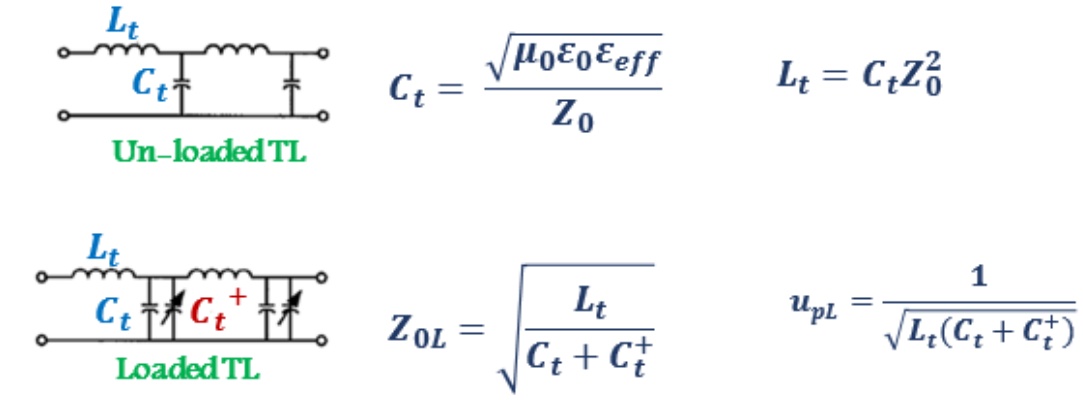


Figure 4-26: Equivalent circuits for loaded/unloaded transmission lines per unit length

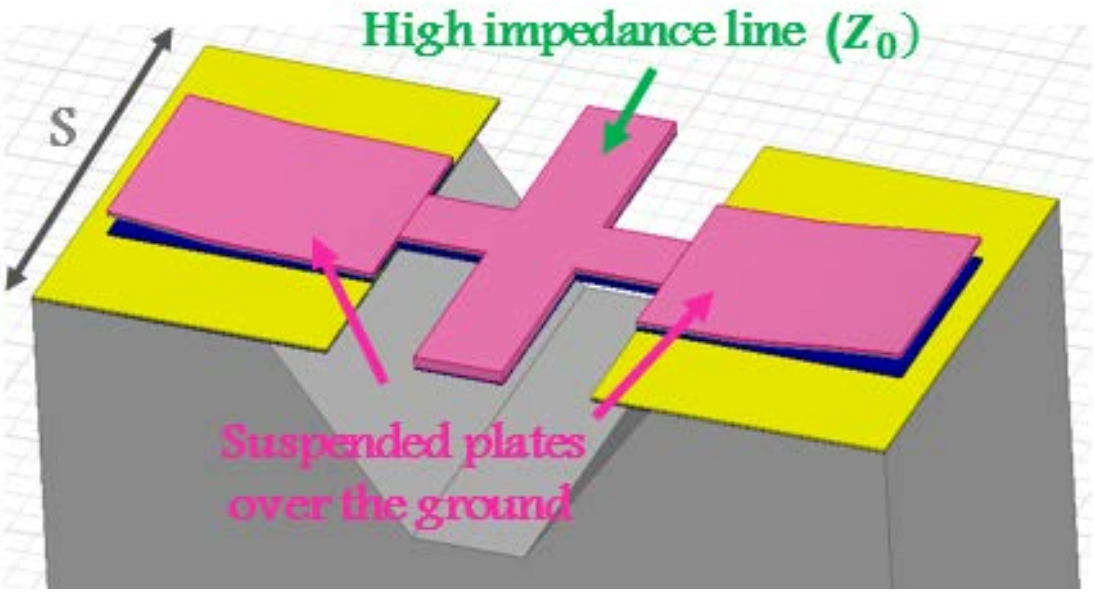


Figure 4-27: Example model of a loaded transmission line segment.

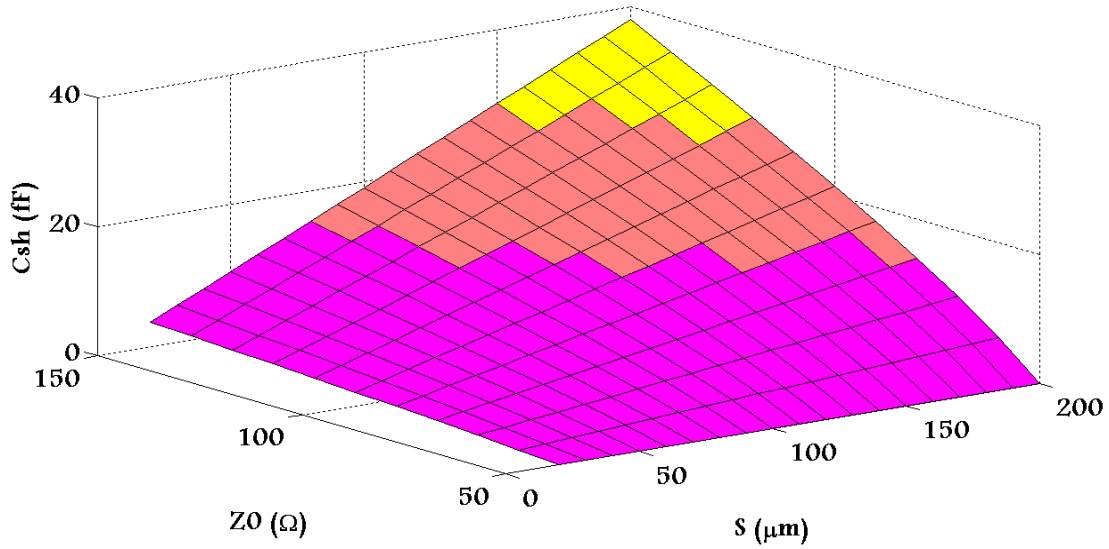


Figure 4-28: Approximate value for shunt capacitor required to match the loaded transmission line section to 50Ω ($C_t^+ = \frac{C_{Sh}}{S} = \frac{2C_{Plate}}{S}$).

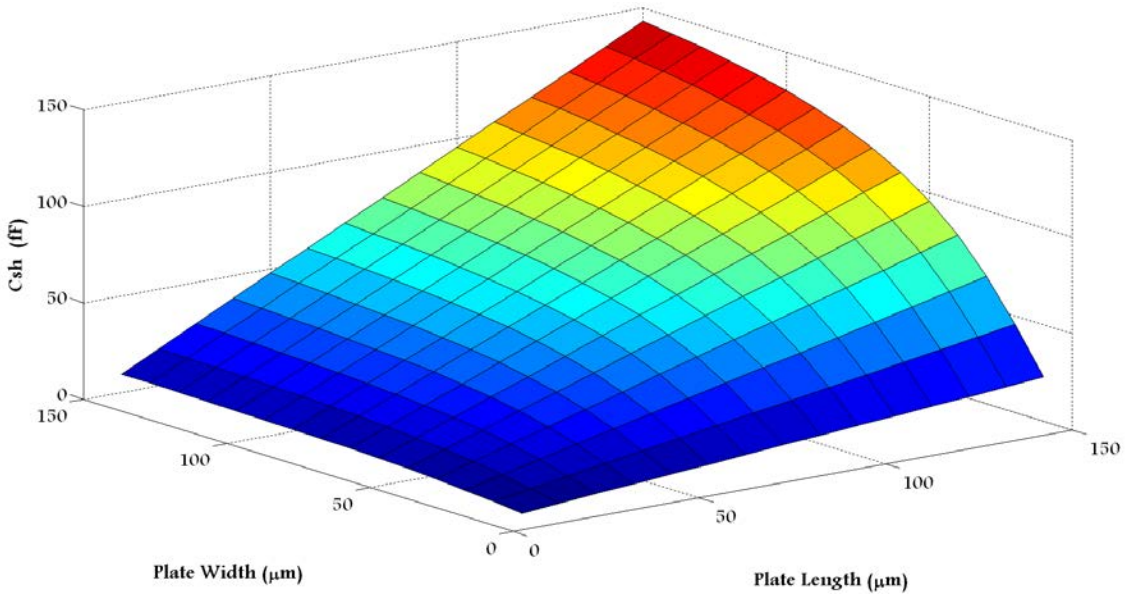


Figure 4-29: Estimated shunt capacitor value associated with two plates based on post-release deflection profile predicted previously.

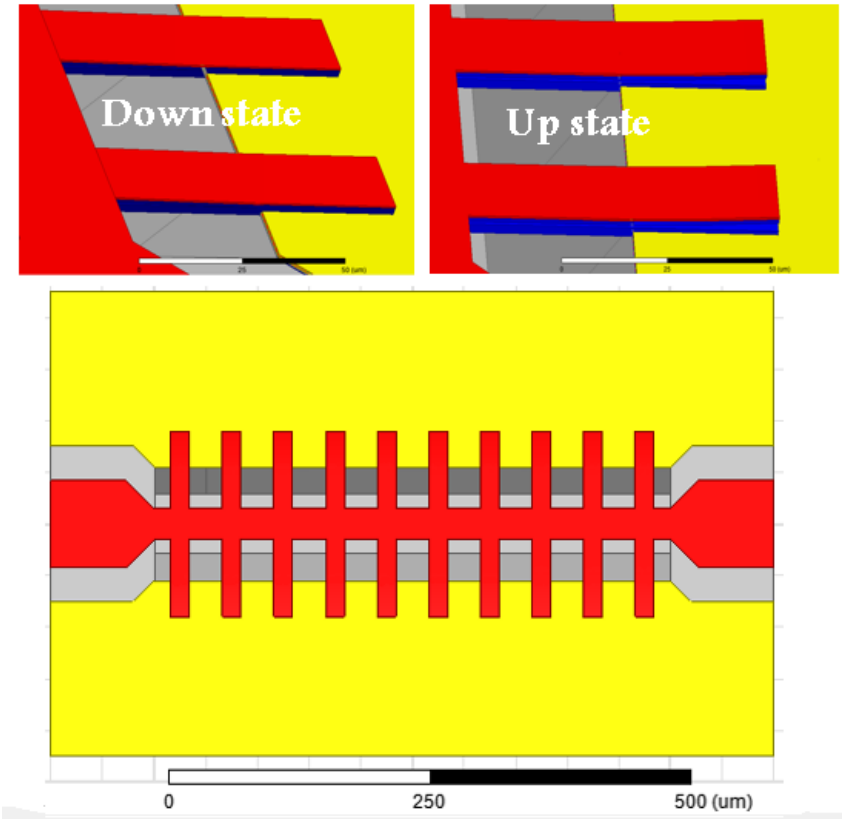


Figure 4-30: Final DMTL circuit model with 10 cascaded sections.

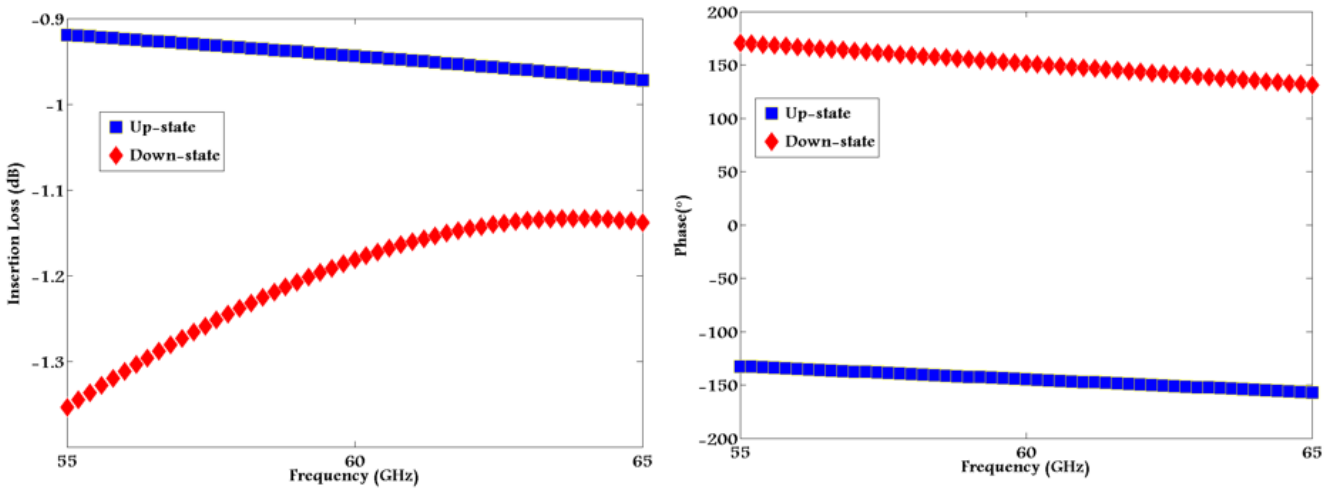


Figure 4-31: Simulation results of the DMTL circuit performance in both states.

Chapter 5
Fabrication Methodology and Results

5.1 Post-processing details and optimized recipes

In this section, we present details of post-processing recipes devised to successfully release MEMS structures on as-received CMOS chips from TSMC. We have employed three RIE machines for the dry etching steps – namely, the Trion Phantom Reactive Ion Etcher at the CIRFE lab, the Oxford Plasma-Lab RIE, and the Oxford Plasma-Lab DRIE at the QNC (Quantum Nano Center) lab, University of Waterloo. The dry etching recipes presented here have been optimized for these RIE systems.

✓ **Cleaning:**

The surface of as-received chips might be contaminated. Cleaning is done by immersion in Acetone, DI water and IPA, respectively. Acetone cleaning can be accompanied by sonication if needed. In some rare cases, depending on the source of the contamination, short immersion in other solutions such as EKC is advised.

✓ **First RIE of oxide:**

Optimized etching recipes for the RIE systems at the CIRFE and QNC labs are presented in Table 5.1. A CHF_3 plasma and a mixture of oxygen and C_4F_8 are used, respectively. The Oxford system has a higher etching rate and is preferred. The samples are loaded inside the chamber on top of a Silicon wafer. For the wafer to be accounted as a thermal sink and to avoid stress build-up in the structures during the first RIE step, the chips are attached to the wafer by a thermal paste. Since the process of etching CMOS dielectric is extremely contaminating, recipe exploiting SF_6/O_2 plasma should be used to clean the RIE chamber.

Figure 5.1 shows images taken by the microscope camera from chip surface prior to and after the first RIE. Observed colors are informative and can be interpreted by experience. The shiny color corresponds to the exposed metal layers, while the regions with a darker color are the areas buried in oxide. Overall, around 6 μm of oxide must be etched to access the substrate. The etching times presented in Table 5.1 are not precise and the chips need to be inspected after each interval of a certain duration to ensure that the desired layers underneath are eventually well exposed. We are cautious to avoid over-timing the process, although the etching is anisotropic. Nevertheless, the oxide side walls, which need to be there to protect structural layers in subsequent steps, could get attacked over time. The chips are taken to SEM for further inspection,

particularly to ensure that the sacrificial metal layer is exposed around the areas where an air gap is to be created (see Figure 5.2).

Table 5-1: Optimized recipe for anisotropic dry etching of oxide (used for the first RIE step).

System	Gas	Flow	Pressure	RIE	ICP	Time	Comments
Trion Phantom Reactive Ion Etcher	CHF_3	50 $SCCM$	20 $mTor$	52 W	200 W	$\approx$ 2.5 h	Plasma ON duration: 5′ Cooling duration: 1′ Chamber cleaning required every 30′
Oxford Plasma-Lab RIE	O_2	15 SCCM	10 $mTor$	200 W	1500 W	$\approx$ 30′	Plasma ON duration: 1′ Cooling duration: 1′ Chamber cleaning required after the process
	C_4F_8	40 SCCM					

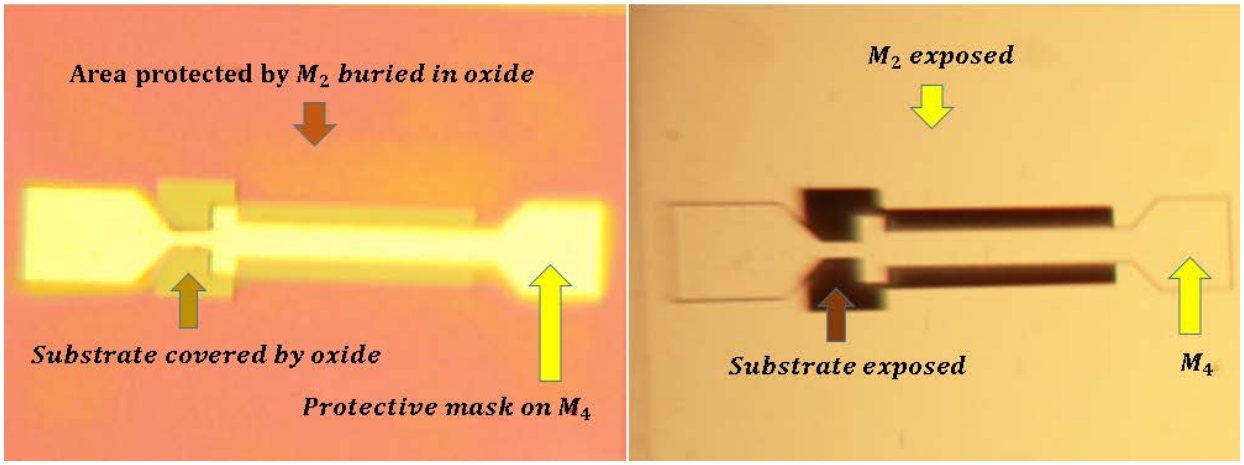


Figure 5-1: Microscope images from a chip prior to (left), and after (right) the first RIE of oxide.

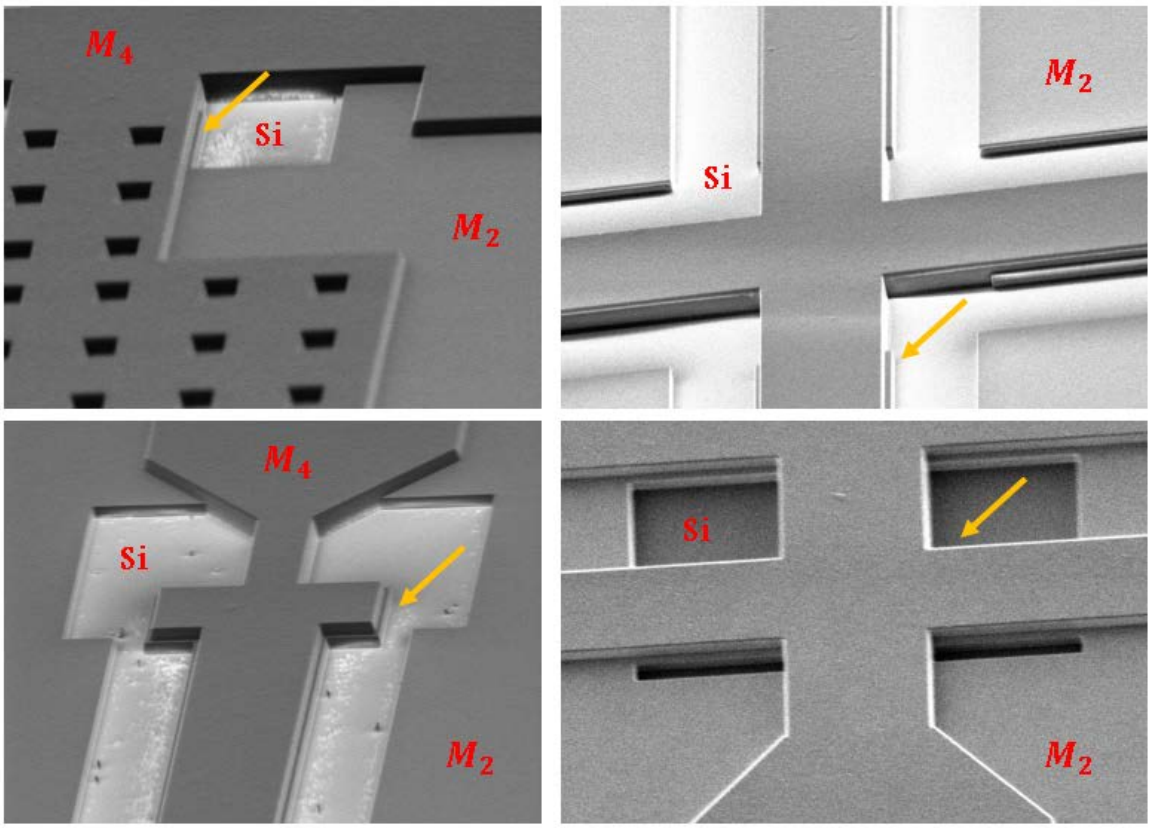


Figure 5-2: SEM pictures after the first RIE of oxide. Areas where sacrificial metal is exposed to create an air gap are pointed by arrows.

✓ **RIE of Silicon:**

Table 5.2 presents optimized recipes for dry etching of Silicon for both systems. The Silicon etch is not fully anisotropic at this step. However, the rate of under-etch can be controlled by adjusting the RIE parameters, particularly the chamber pressure (higher pressure results in a deeper undercut). The values required for the depth and undercut of the trench are determined from RF simulation and can be realized by adjusting the pressure and duration of the etching. In the simulation phase the presumed values for the air trench depth and Silicon under-etch were $\approx 60\ \mu m$ and $\approx 20\ \mu m$ respectively. To avoid damage or stress build-up in the samples, we do not recommend exceeding the power values given in the table. The chips need to be inspected every 10 minutes. Figure 5.3 shows SEM pictures of areas from which the undercut depth can be estimated. Figure 5.4 displays the chip at the end of the Si RIE stage.

Table 5-2: Optimized recipe for isotropic dry etching of Silicon.

System	Gas	Flow	Pressure	RIE	ICP	Time	Comments
Trion Phantom Reactive Ion Etcher	SF_6	40 $SCCM$	50 $mTor$	50 W	-	$\approx 45'$	✓ Plasma: $1'$ ✓ Cooling: $1'$
Oxford Plasma-Lab DRIE	SF_6	160 $SCCM$	15 to 20 $mTor$	20 W	1000 W	$20'$ to $30'$	✓ Cycles of $10'$ chamber cleaning after the process

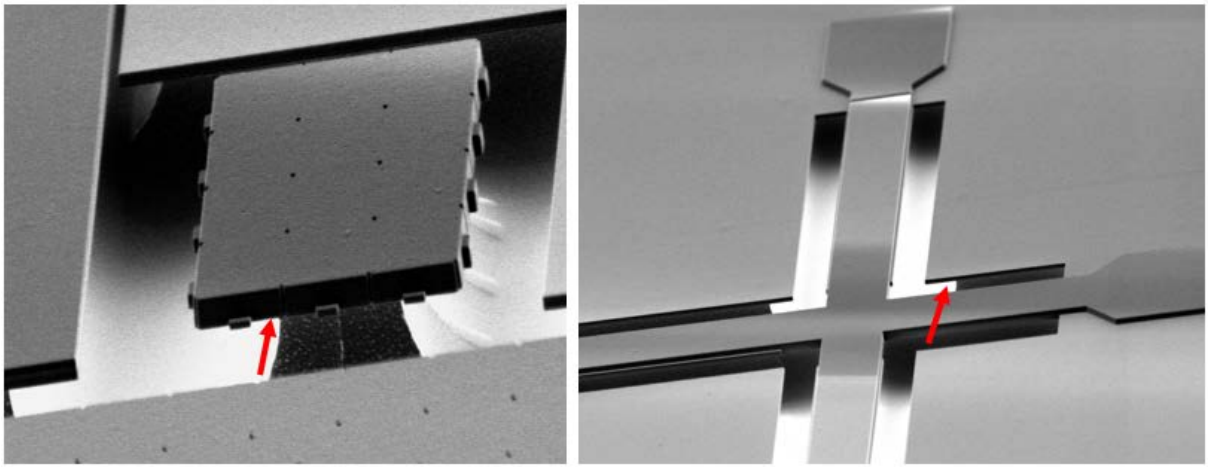
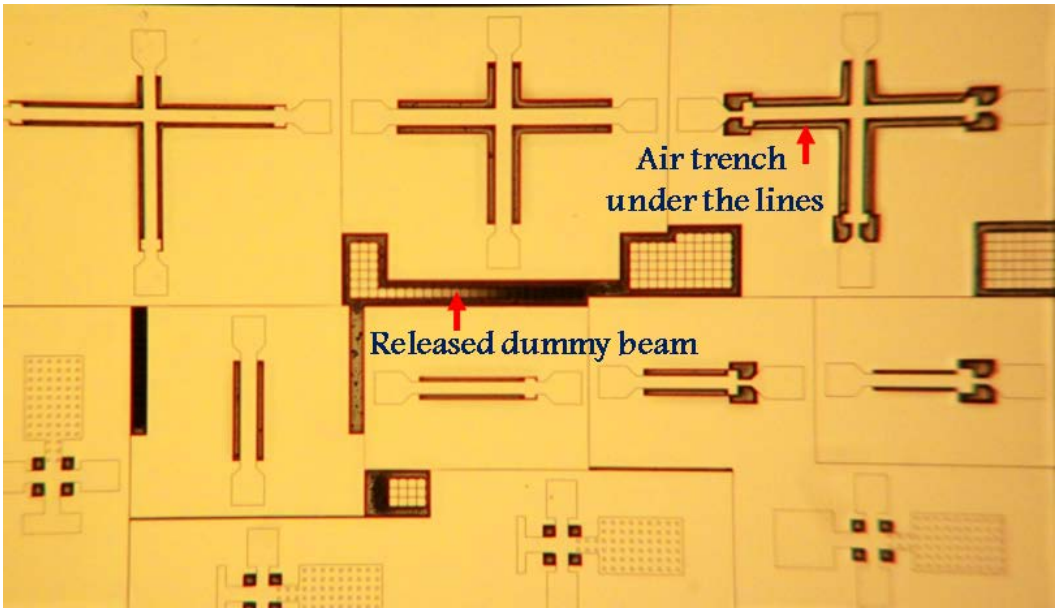
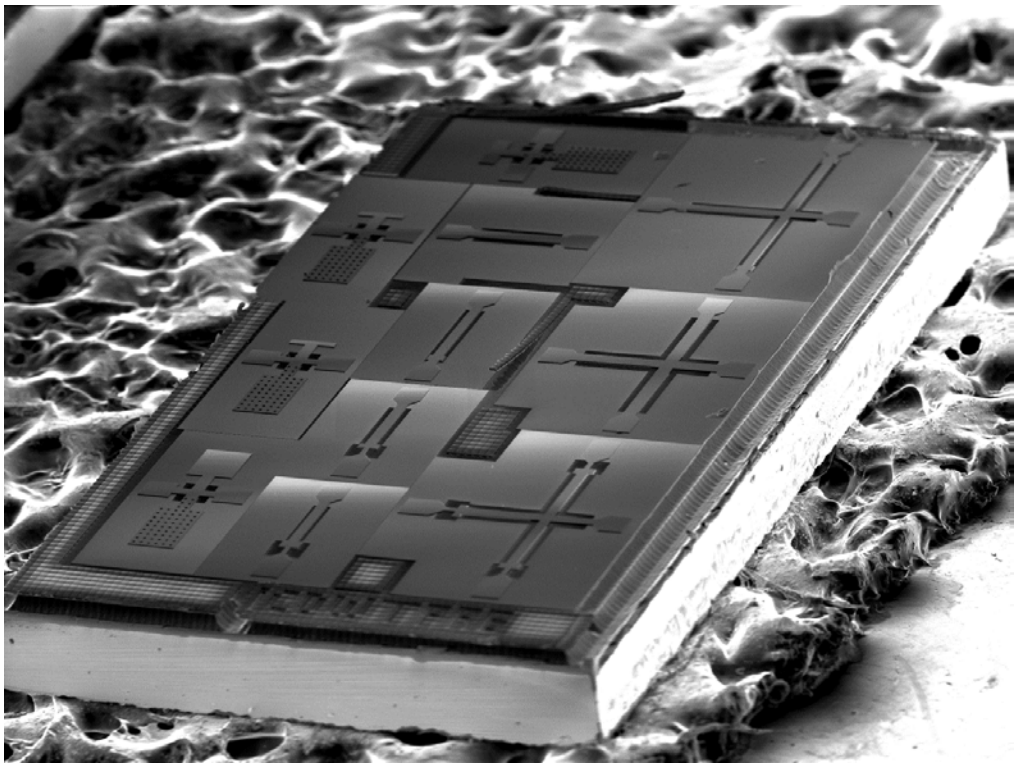


Figure 5-3: Estimating Silicon under-etch from SEM pictures.



(a)



(b)

Figure 5-4: Chip after RIE of Silicon, image from (a) microscope camera, and (b) SEM.

✓ **Wet etching:**

In our experience, the last two steps of post-processing (namely, the wet etching and the 2nd RIE of oxide) are the most challenging ones. The wet etching step includes immersion in EKC, PAN, H_2O_2 and KOH solutions with the recipes presented in Table 5.3. The goal is to remove the post-RIE polymer, etch away the sacrificial metal layer and protective mask, remove the thin adhesion TiN coating underneath the metal, and finally clear off the air trench from the piles of remaining Silicon. At the end of the wet etching, to avoid release stiction, supercritical CO_2 drying is essential. Chips need to be immersed in pure IPA petri dishes a few times before being loaded in a CPD chamber filled with IPA.

Table 5-3: Optimized wet etching recipe

Material to be removed	Solution	Dilution	Temperature	Time	Comment
Post RIE polymer	EKC	-	65°,	$30'$	✓ Cold loading in a shallow petri dish ✓ Immersion in DI water at least twice prior to each step
Aluminum	PAN	16:1:1	40°	$60'$	
TiN	H_2O_2	30%	40°	$30'$	
Silicon	KOH	60%	40°	$60'$	

It is important to ensure that the sacrificial metal is well-exposed to the etchant solution and entirely cleared off. If the sacrificial area on M_2 is wide, the top metal layers (M_3 and M_4) must have reasonably large release holes to facilitate the wet etch. Figure 5.5 is a snapshot from M_3 and M_4 layouts for a plate to be released, showing optimized values for release holes width and spacing.

As soon as the protective top metal is gone and an air gap is formed, the samples are extremely vulnerable. The beam and plates can be easily damaged or even totally peeled off by mishandling, flipping or collision. That is why, although etching at higher temperatures is obviously faster and more effective, we experienced that we should use maximum 40° for the last three steps mentioned in Table 5.3. At higher temperatures, the chips might scatter around and hit the side walls. Especially during the KOH step, the reaction usually forms bubbles around the chips that could result in turning and flipping. We also learned by experience that cold loading leads to better stiction of the chips to the bottom of the petri dish for the entire duration.

It is important to keep in mind that KOH attacks oxide as well, although the etching rate is not significant. Therefore, a longer immersion time in KOH translates to a thinner oxide between the plates, as the thickness of D_3 and D_2 is being decreased. It can be shown by mechanical analysis of the bi-layer beams that a thinner

oxide leads to a higher stress-induced post-release deflection. This may or may not be favorable for some designs. Moreover, another risk of a prolonged KOH etch is the Polysilicon line underneath M_1 getting exposed and attacked. This would disconnect the bias line and make DC actuation impossible. Considering all of the above, this last step of immersion in KOH can be skipped in some cases. However, the recipe for RIE of Silicon needs to be adjusted to be more isotropic in order to create a deep air trench without excessive undercut.

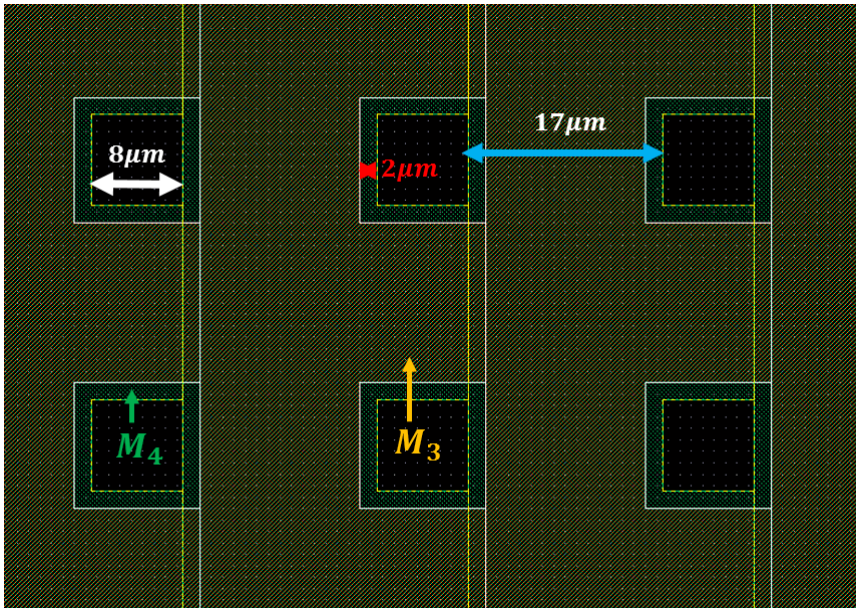


Figure 5-5: Optimized release hole dimensions on M_3 and M_4 for a successful wet etch of the sacrificial layer on M_2.

Figure 5.6 shows SEM pictures of some structures after the wet etching step in which the narrow air gap created by sacrificing M_2 is noticeable. At this stage, since metal beams and plates are sandwiched between oxide layers on both sides, upward warpage is not yet expected.

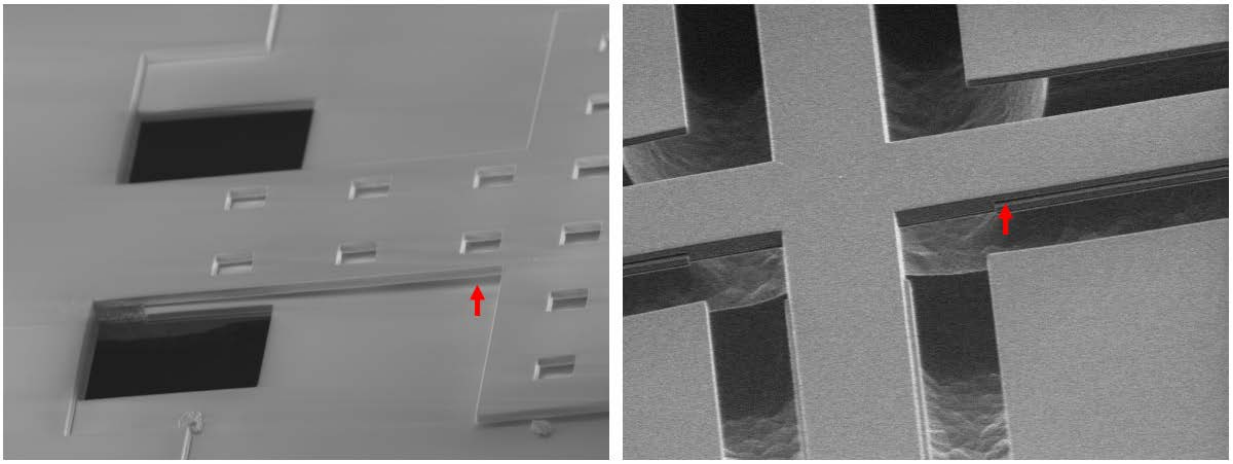


Figure 5-6: SEM pictures after the wet etching step, with arrows pointing at the created airgaps.

✓ The second RIE of oxide:

At this stage, the chips are entirely covered with an oxide layer ($\approx 1\mu m$) that should be fully removed to uncover the pads for a proper probe contact and to enforce the desirable upward warpage of the released bi-layer beams/plates. The final deflection profile that determines the RF performance of the circuit is highly dependent on the etching condition. Therefore, the recipe for the second RIE of oxide has to be optimized and cannot simply be similar to the one in the first post-processing step. In addition to the residual stress mismatch, the RIE plasma itself contributes to thermal stress in structures. The components are extremely delicate at this point and likely to be damaged by over-etching or by excessive thermal stress during heating or cooling cycles. We experienced that the inherent residual stress of as-received CMOS chips might vary from one tape-out to another and might not always be enough to provide the desired deflection profile required to achieve a high capacitance ratio. Therefore, following the advice suggested in [74], we strove to enhance the thermal induced stress carefully by optimizing the duty cycle and RIE power.

Table 5.4 gives the optimized recipe that would provide very large upward deflection for the beams and plates. The main trick was to avoid using the typical adhesive thermal paste to attach the chips to the wafer, and to increase the RIE power significantly in comparison with what we normally used for oxide etch. The etching duration, however, has to consist of very short cycles of 20 seconds, with 8 to 12 cycles being needed overall. Furthermore, the chips need to be inspected by microscope to ensure that the pads are

uncovered and adequate deflection is achieved. For the deflected plates or beams the tips would be out-of-focus when inspected by microscope (see Figure 5.7).

Table 5-4: Recipe for second RIE of oxide optimized to create enhanced deflection by inducing proper thermal stress.

System	Gas	Flow	Pressure	RIE	ICP	Time	Comments
Oxford Plasma-Lab RIE	O_2	15 SCCM	10 $mTor$	200 W	2500 W	$160''$ to $240''$	✓ Plasma ON: $20''$ ✓ Cooling: $20''$ ✓ No thermal paste
	C_4F_8	40 SCCM					

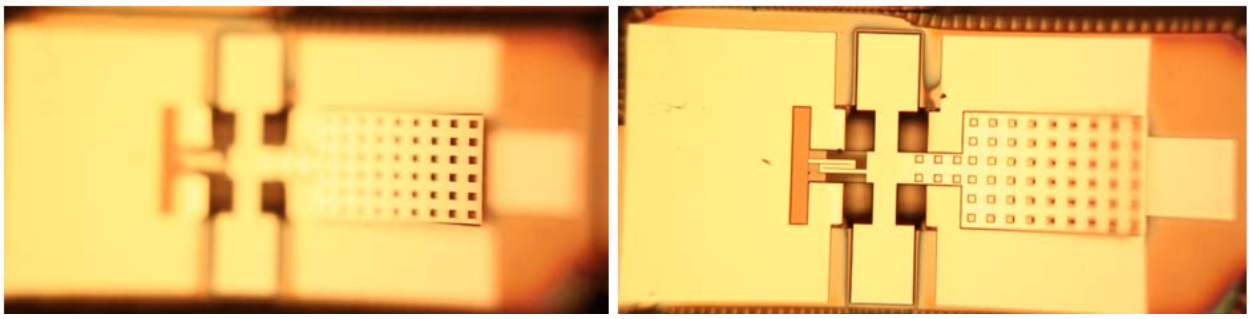


Figure 5-7: Inspection of released plates by microscope. Deflection is evident when plates are partially out of focus.

5.2 Fabricated CMOS-MEMS devices

The designed structures presented in Chapter 4 were all translated into appropriate layout files consistent with TSMC design rules for CMOS 0.35 µm. The layouts were then submitted to TSMC for fabrication. The optimized post-processing procedure presented in 5.1 was employed to release the desired MEMS components from the CMOS chips. In this section, we present SEM pictures of successfully fabricated circuits ready for RF measurement and DC actuation.

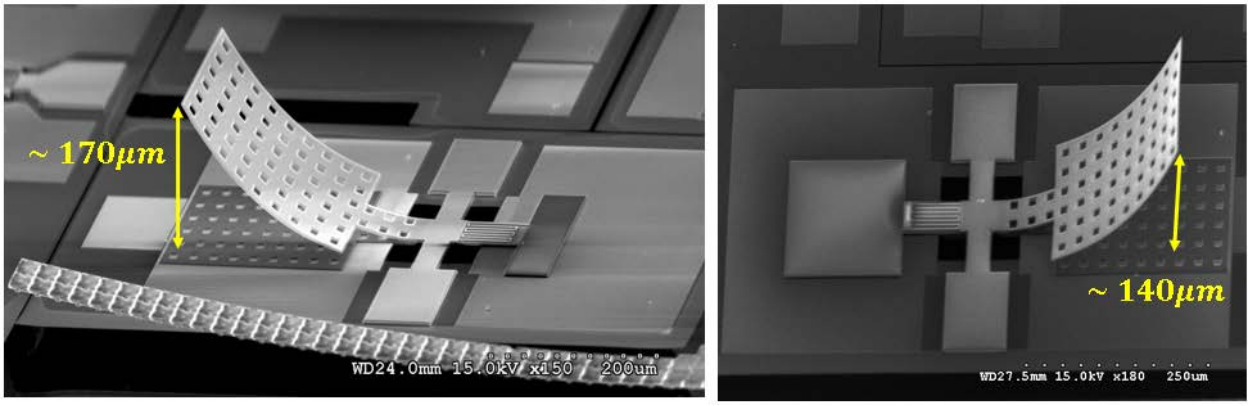


Figure 5-8: Variations of normally-ON SPST switches designed for 60 GHz released with high warpage.

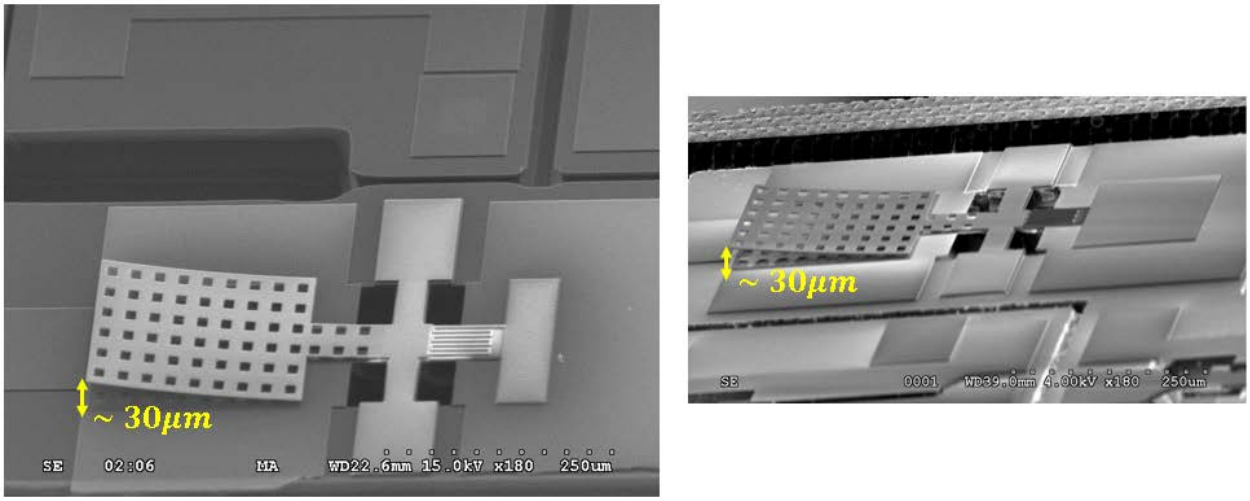


Figure 5-9: Variations of normally-ON SPST switches designed for 60 GHz released with low warpage.

Figure 5.8 shows normally-ON SPST switches that were designed to operate at 60 GHz. The plates are released using the special second RIE recipe presented earlier in Table 5.4. The post-release deflection is almost 3 times higher than the value presumed at the simulation stage (CoventorWare analysis predicted tip deflection of $55\mu m$) . Referring to Chapter 4, where we explained the design strategy of the normally-ON switches, we would, with a lower Up-state capacitor, expect matching to occur at a higher frequency. Designs in Figure 5.9 which have been processed differently (not using the optimized second RIE recipe) ended up with small tip deflections (less than the predicted value). We would expect the center frequency to shift down. It is evident from Figure 5.9 that the inherent residual stress is insufficient to provide the desired warpage.

As explained in chapter 4, for normally-OFF switch circuits, extreme upward deflection is advantageous to Up-state isolation with no effect on the ON-state performance or operation frequency. Figure 5.10 shows 60 GHz SPST normally-OFF designs released with a high tip displacement. Beams with medium and low deflections are shown in Figure 5.11. The SP3T switch designs are the most fragile, for having three suspended beams anchored at a point, and are therefore less likely to survive post-processing. Figures 5.12 and 5.13 show several successfully released ones with different deflection profiles ready for RF measurement. Figure 5.14 shows the DMTL structure designed for 60 GHz with ten pairs of beams in series. For this structure, an extreme beam warpage is not desired or the Up-state matching of the circuit would be disturbed.

Circuits have been tested for actuation by a pair of DC probes connected to a DC power supplier (Figure 5.15 shows the device under test and the probes). The plates in normally-ON switch structures were pulled down by at most 80 V applied between the CPW line and ground plane (the CosolveEM analyzer of CoventorWare software had predicted the pull-in voltage to be 66 V for a warped plate with 55 μm tip deflection). The required pull-down voltage was higher for the beams in normally-OFF switch designs. Voltage applied between the main line and the actuation electrode had to be in the range of 100-200 V to snap the beam.

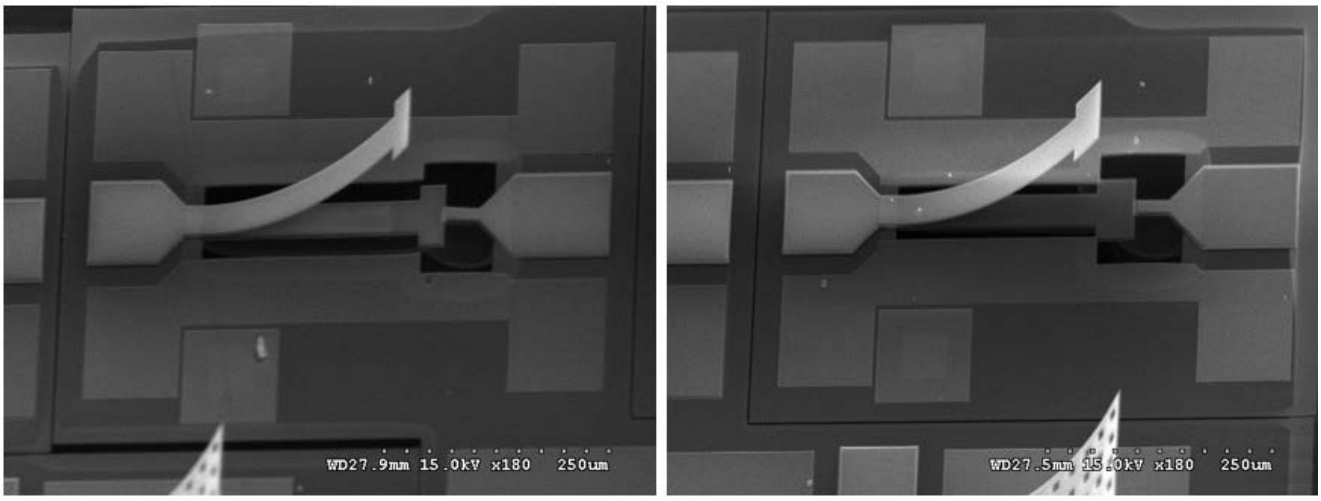


Figure 5-10: Variations of 60 GHz normally-OFF SPST switches released with high warpage.

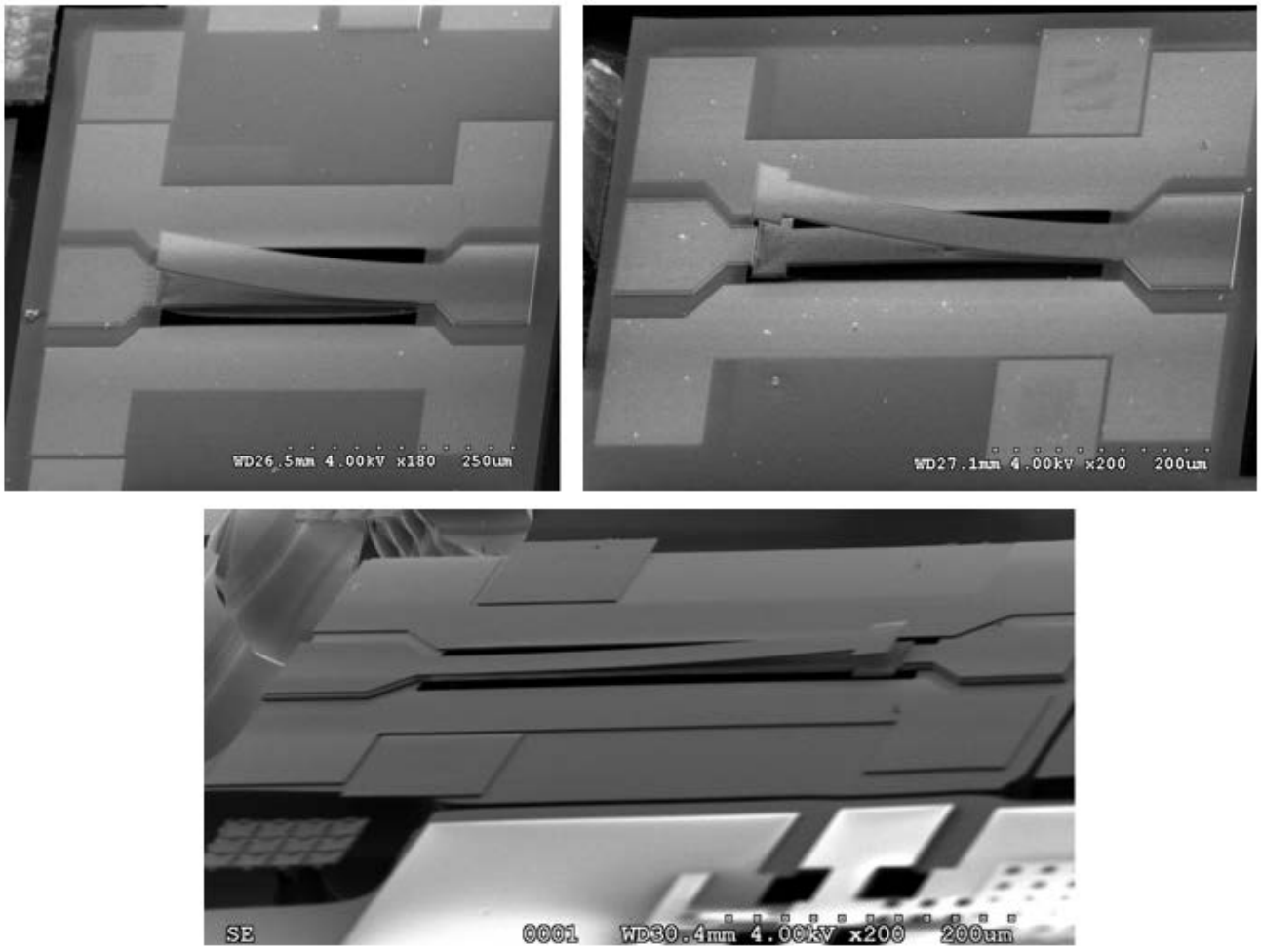


Figure 5-11: Variations of 77 GHz normally-OFF SPST switches released with medium or low warpage.

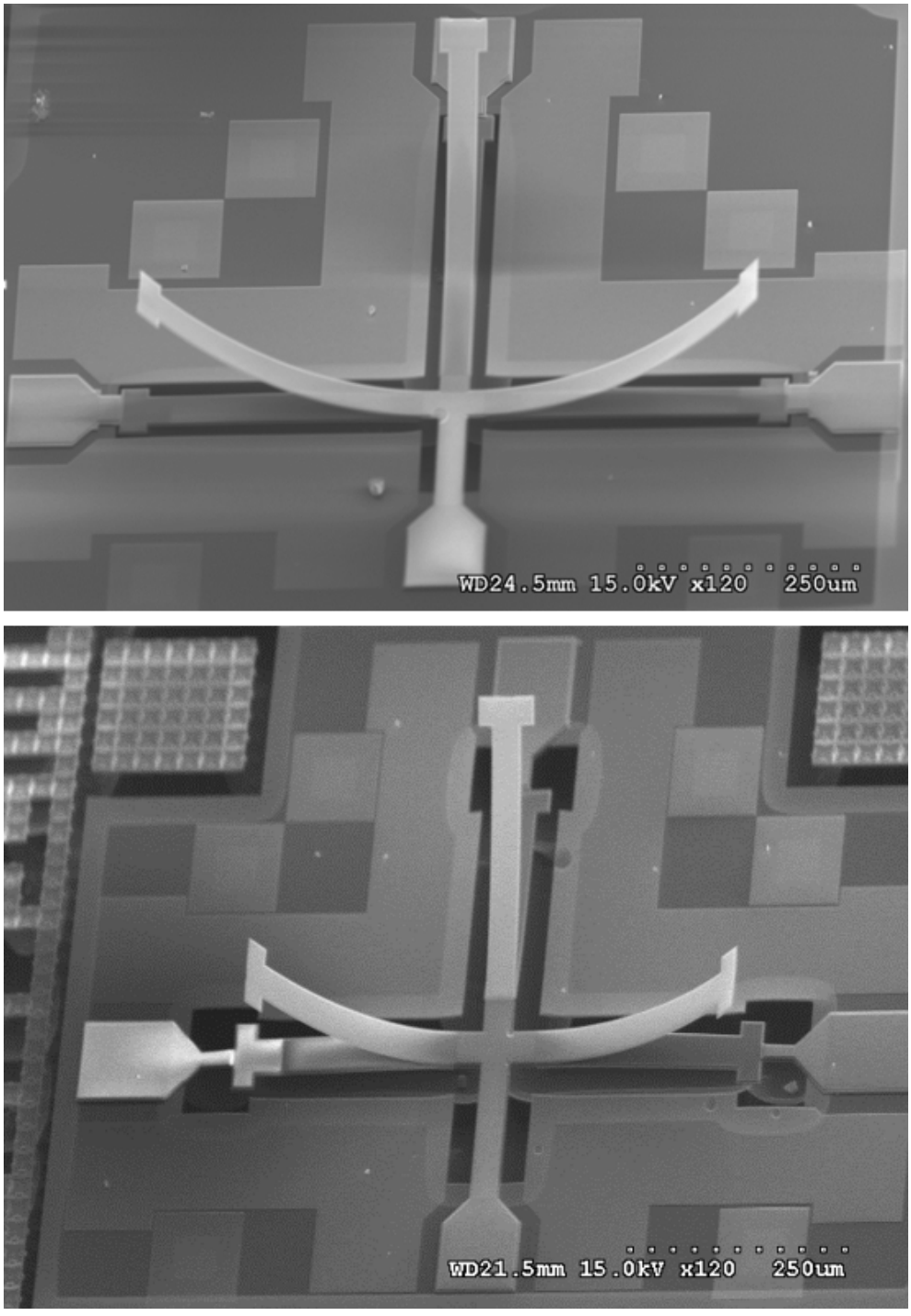


Figure 5-12: Normally-OFF SP3T switches designed for 77 GHz (up) and 60 GHz (down), both released with high warpage.

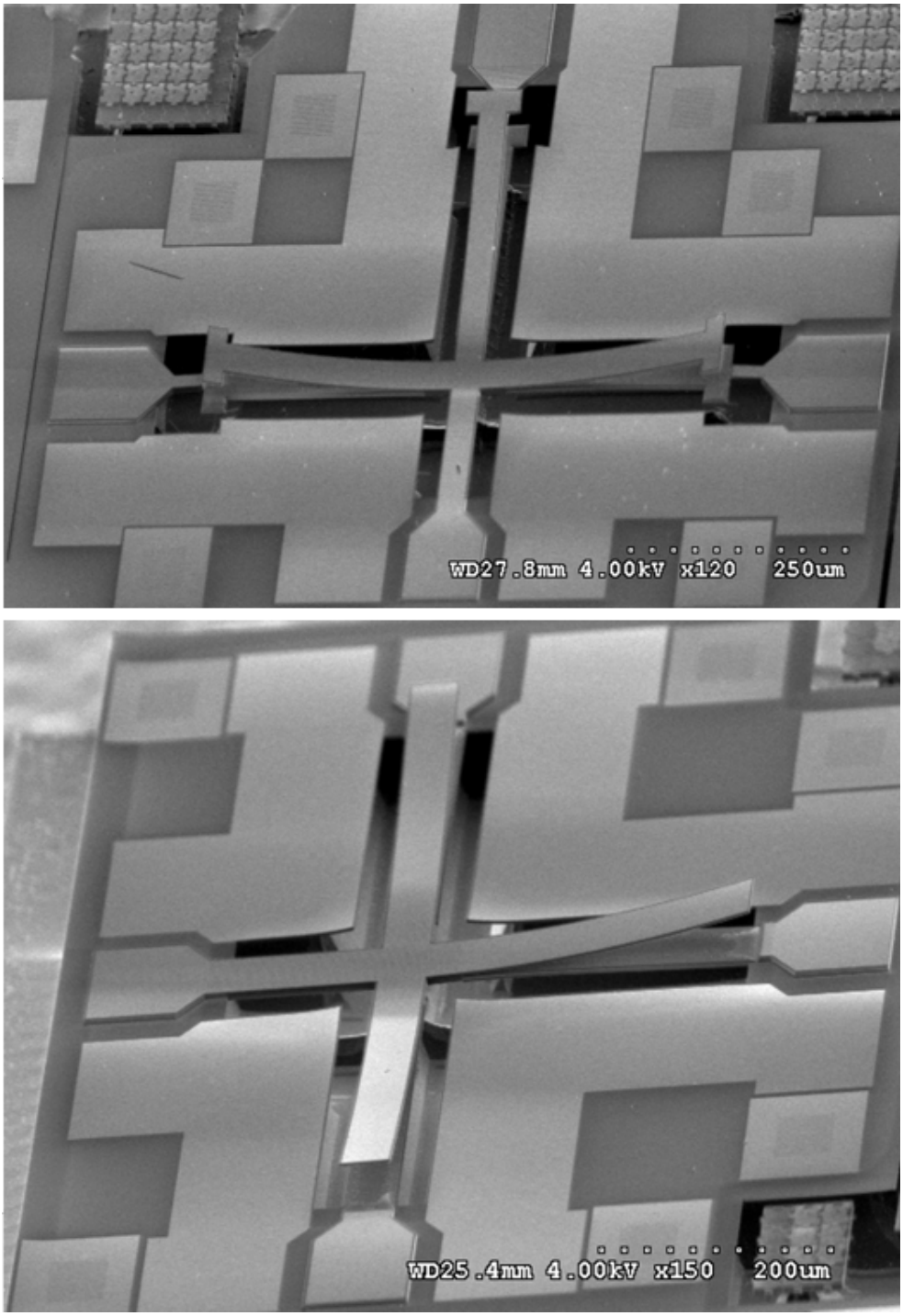


Figure 5-13: Normally-OFF SP3T switches designed for 60 GHz (up) and 77 GHz (down), both released with medium warpage.

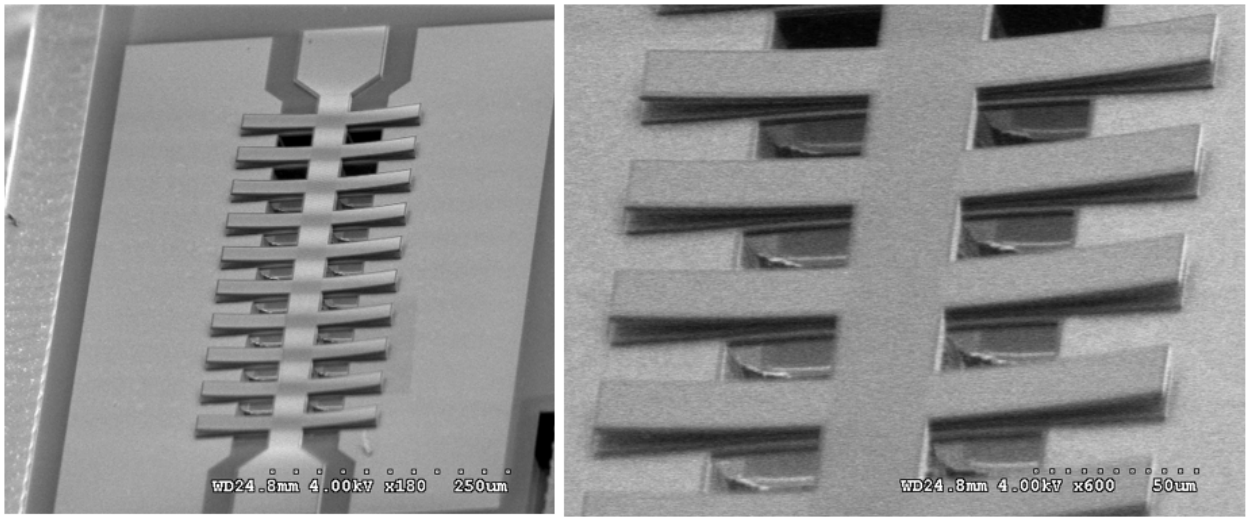


Figure 5-14: SEM pictures from a released 60 GHz DMTL structure.

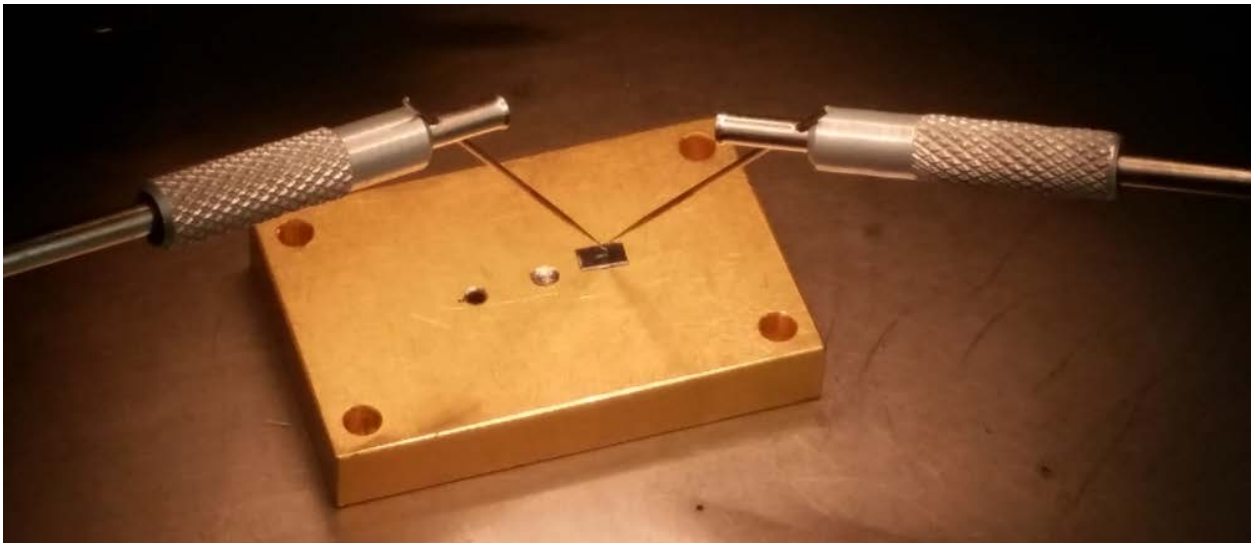


Figure 5-15: Actuation test by DC probes.

Chapter 6
Conclusion

6.1 Summary of thesis

- In this thesis, we studied the integration of MEMS on CMOS by means of post-CMOS techniques to create MEMS components from patterned BEOL layers of CMOS technology.
- The BEOL layers of TSMC 4M2P CMOS 0.35 μm technology (Aluminum and Oxide layers) were used to design several RF-MEMS reconfigurable components. Electrodes connected to DC pads via high resistivity Polysilicon bias lines were employed for electrostatic actuation.
- All circuits were based on EC-CPW transmission lines and were designed and optimized to operate at mm-wave frequencies of 60 GHz or 77 GHz with a bandwidth of 10 GHz.
- Challenges had to be dealt with to meet matching requirements at high frequencies.
- Designs were optimized within the constraints enforced by the material properties of the CMOS technology as well as limitations dictated by the post-processing method.
- A mask-less post-processing procedure that included several dry and wet etching steps (previously developed at the CIRFE lab) was precisely optimized and conducted to successfully release the desired MEMS circuits from CMOS chips received from the foundry.
- It was shown how post-processing conditions could be optimized to enhance switch performance, by enhancing the post-release deflection profile of the beams and plates to achieve a better figure of merit in terms of the capacitance ratio between the states.
- The following CMOS-MEMS reconfigurable circuits were designed and fabricated:
    - ✓ Variations of 60 GHz and 77 GHz SPST normally-ON shunt capacitive switches with released plates and upward deflection suspended over CPW ground plane, designed to provide matching at the center frequency. The switches turn OFF by electrostatic actuation of the MEMS plates (up to 80 V would be required). Simulated ON-state insertion loss of the normally-ON SPST switch was less than 1.8 dB including the loss from the RF measurement pads and the effect of lossy CMOS materials. Switch dimensions (including RF and DC pads) were approximately 350 μm by 750 μm.
    - ✓ Variations of 60 GHz and 77GHz SPST normally-OFF series capacitive switches in which the CPW line itself consisted of a released deflected beam with a capacitive coupling to the other

side of the circuit. The switches turn ON when the beams are actuated (100-200 V is required for pull-in). Simulated ON-state insertion loss was around 1 dB, with OFF-state isolation of at least 20 dB. Circuit dimensions were approximately 400 μm by 550 μm.

- ✓ SP3T switches made from three normally-OFF series capacitive switches and cross junctions. The simulated insertion loss of a connected path in the SP3T switch was better than 1.5 dB and isolation for the disconnected branches was better than 25 dB. Dimensions were around 700 μm by 950 μm.
- ✓ A 60 GHz DMTL circuit on CPW line loaded with switchable shunt capacitors acting as a single bit phase shifter. The circuit was around 300 μm wide and expected to provide an approximate phase shift of 60° per each 100 μm line length, when capacitive plates were actuated. The simulated insertion loss (including the loss from the RF measurement pads) was less than 2 dB for both operation states.

6.2 Challenges and future work

In this section, we review a list of challenges with the design and fabrication of CMOS-MEMS capacitive reconfigurable components using the post-CMOS process presented in the thesis. Future work could focus on addressing the following issues:

- It is well-known that capacitive switches have a narrower band in comparison with contact switches. One limitation with the current post-processing method is that the oxide underneath the released metal layers cannot be discarded, so the metal-to-metal contacts could not be realized by this fabrication approach. Innovative ideas could be investigated to come up with more flexible post-CMOS fabrication methods.
- One major concern for designing any RF-MEMS capacitive switch is the lifetime limitation due to stiction and dielectric charging effects. It is important to optimize the anchored bi-layer beam size to obtain reasonable stiffness and provide sufficient restoring force to bring up the plate when the actuation voltage is OFF.
- The switching time, which could matter for some applications, depends on the mechanical response of the actuator as well as the DC bias routing. The long and narrow high resistivity Polysilicon lines that have been used for biasing our circuits (to prevent DC current formation) introduce a high RC delay

and slow down the switching. A comprehensive analysis would be required to predict and optimize the switching time.

- The surface roughness of the oxide, which hinders the formation of a full contact, has not been taken into account in simulations. Thus, the Down-state capacitance is less than predicted. One solution would be to increase the immersion time in KOH and slightly decrease the oxide thickness to enhance the Down-state capacitance and decrease the Up-state capacitance (due to the resultant higher post-release deflection) simultaneously. This could improve the figure of merit for the capacitive switch.

6.3 Potential applications

There are numerous potential applications for the mm-wave CMOS-MEMS components presented in this thesis. The implemented SPST switches proposed in this work could be employed as basic building blocks for more complicated multiport multistate compound switches, such as C-type, R-type and T-type switches. One example is the T-type configuration illustrated in Figure 6.1, which can be constructed using SPST switches along with transmission line turns and junctions. Another application of the presented SPST switches would be in switch cells of matrices, which are required for signal routing when system redundancy is to be achieved. Figure 6.2 shows a widely used multi-input/multi-output crossbar switch matrix cells which can be implemented by two pairs of SPST switches in combination with junctions and cross-overs.

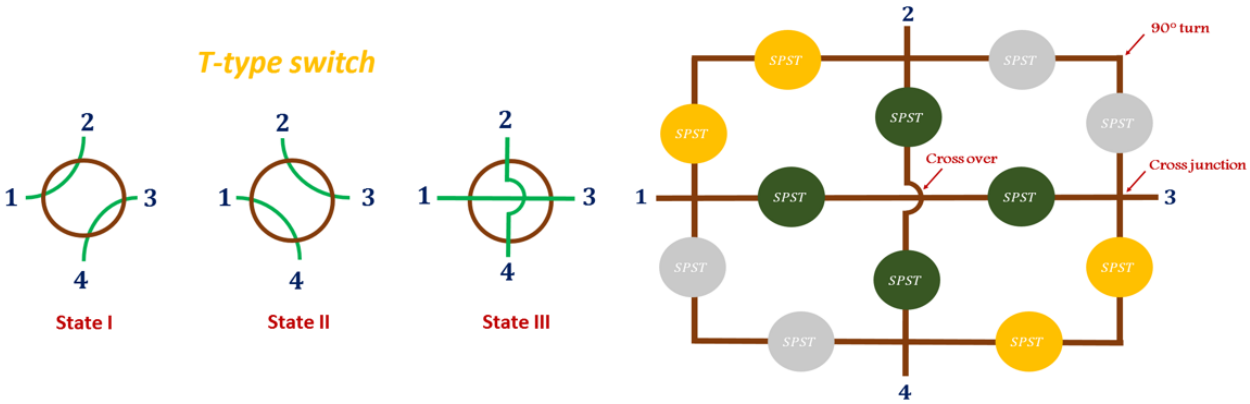


Figure 6-1: Compound multiport T-type switch as potential application of SPST switches proposed in this work. Possible states and circuit configuration are shown. For each of the three operational states, one group of four SPST switches (shown here with the same color) should be simultaneously actuated.

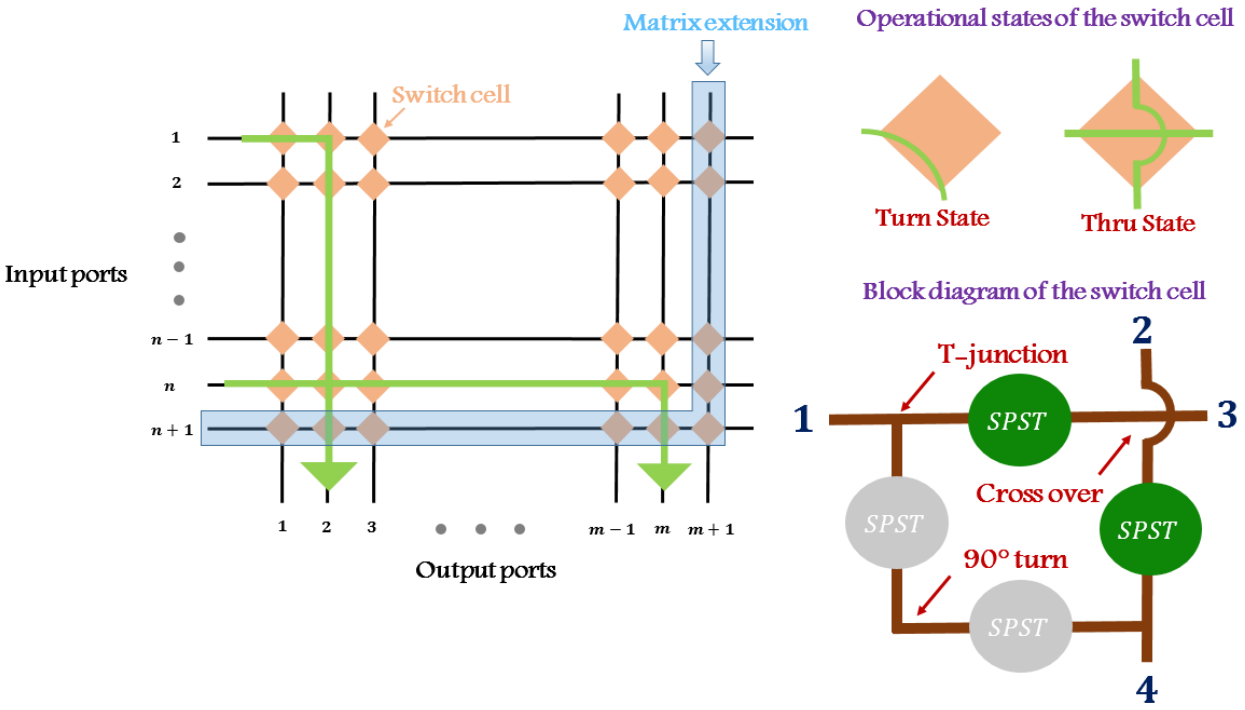


Figure 6-2: Switch matrix used for signal routing as potential application for SPST switches proposed in this work. For each operational state of the constructing switch cells, a pair of SPST switches (shown in the same color) are simultaneously actuated.

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